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INSTRUCTIONAL MANUAL

VECTOR COMPONENT COMPUTER

MODEL 202 and MODEL 202A

DRANETZ
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INDEX OF SCHEMATIC DIAGRAMS

	Assembly No.	Drawing No.
A/C Ampl	100717B	A100719
F-F	100720B	A100722
S.P.I.	100723A	A100725
D.S.D.	100726B	A100728
S.S.S.	100729A	A100731
G.S.D.	100732A	A100734
Z.C.D.	100735B	A100737
S & H	100775A	A100882
E.F.	100774A	A100883
Bridging Unit	100713A	B100710
C.P. Function Chart	100746	B100746
Sig., Sw. & Aux. Ckts. P.S.	100761B	C100763
Rear Panel Wiring (2 sheets)	-------	C100745
Wiring Diagram, Plug-in Con.....	-------	C100745
Power Emitter Follow, Plug-In	Model 202-PA-2501	C100705
Gate Ckts. (2 sheets)	-------	C100743
Comp. Elem.	-------	C100740
Front Panel (202only)	--------	C100884
Timing & Output Ckts. (2 sheets)	100747B	C-F100749
A.C. Limit Circuits	100753B	D100755
Front End Circuits	100756B	F100758
Pwr. Em. Foll.	-------	B100247
Front Panel (202A only)	-------	C101179
Signal Ckts. P.S. Assy	100759	FAB100759
Plug-In P.S. Assy	100761	FAB100761

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LIST OF SCHEMATICS FOR COORDINATE CONVERTER

(Used in Model 202A Only)

Coordinate Convertor Schematic	C 101151
Parts Layout:	
Rear View	B 101160
Ckt. Board Assy.	B 101162
Input Stage	A 101159
Meter Switch	A 101158
Oscillator	A 101157
Chopper Driver	A 101156
Detector	A 101155
Differentiator	A 101154
Regulator +18V D.C.	A 101153
Regulator -18V D.C.	A 101152
Voltage Source	A 101161

SECTION I

1-1 INTRODUCTION

The Vector Component Computer Model 202 is an instrument which provides D.C. outputs proportional to the in-phase vector component, and the quadrature vector component of a 0 to 30 millivolt rms signal input, using a second signal of 3 volt rms for phase and amplitude reference. The Model 202A in addition to in-phase and quadrature outputs provides magnitude and angle simultaneously.

Plug-ins and adapters of the 100-PA and 202-PA-series may be used for the measurement of impedance, admittance, transfer function, etc., under CW or pulsed CW (tone burst) conditions of test sample drive.

The Vector Component Computer is built in an 8 3/4" high, by 17" wide, by 16" deep enclosure. It can be rack mounted by the use of any standard chassis slides which will accept a 17" wide chassis.

A front panel opening is provided for installation of the function determining plug-ins and adapters. The 202-PA-series units plug directly into the front panel. A bridging unit is supplied for use with the much smaller 100-PA-series units.

A rear panel opening is provided for special purpose plug-ins in the 202-PAR-series. An Emitter Follower plug-in Model 202-PAR-2501 is supplied for use with the 100-PA-series low power plug-ins, it will provide 3 V RMS into a 40 Ω load.

1-2 Accessory Equipment Required

A. Output Readout Devices

The Vector Component Computer has no output meters. External D.C. meters, an X-Y recorder or some other D.C. indicating or recording devices are required for information readout. The Real channel output is normally a 0 to +5 volts D.C. signal although it may vary from -5 to +5 volts with differential type Z to Y plug-ins and transfer function plug-ins. The Quadrature channel output normally varies from -5 to +5 volts D.C. regardless of plug-in type. For the Model 202A only, 0 to 1 V full scale output is provided for vector magnitude and a 0 to + 1.8 volt output for 0 to + 180° vector phase. The readout devices should have an input impedance of 10KΩ or larger. (See Table 2 for D.C. output connector pin functions.)

1-2 Accessory Equipment Required (continued)

B. Reference and Information Signal Monitoring Equipment

The Vector Component Computer does not require a precise control of the nominal 3 volt reference signal when used with 100-PA or 202-PA-series plug-ins. Variations of + 20% are automatically compensated for within the Vector Component Computer. Front panel lights indicate any out-of-limits operation and also when correct computation has been performed by the Vector Component Computer.

In CW operation, an A.C. meter may be connected to the 202-PAR-2501 EXT. AMPL. INPUT jack to monitor the reference signal. When this plug-in is not used, the reference signal may be monitored at the AUX. EQUIP. connector on the Vector Component Computer rear panel. (See Table 2 for pin connections.)

In tone burst operation, an oscilloscope is required for monitoring Vector Component Computer input signals. Both the Reference and Information signals are scaled within the Vector Component Computer to approximately 3 volts peak to peak, and are available at the A.C. OUTPUT connector on the rear panel. (See Table 2 for pin connections.) It is necessary to observe both reference and information signals during tone burst operation since turn on and turn off transients may obscure the desired data. To assist the operator in determining if the Sample Time and Sample Delay are adjusted properly, both AC output signals have a pedestal applied. The pedestal corresponds to the total time interval required by the Vector Component Computer to properly compute the desired information.

C. Oscillators, Amplifiers, and Signal Sources

1. CW operation with low power 100-PA-series plug-ins.

If the impedance of the test sample is greater than 40Ω (less than 25K micro mhos) the 202-PAR-2501 may be used to provide the drive signal for the test sample. An oscillator capable of at least 3.5 volts rms into a 5 KΩ load over the frequency range of test is required. Connect the oscillator to the OSC. INPUT jacks on the 202-PAR-2501. The oscillator must have less than 0.5% distortion. If the test sample impedance is less than 40Ω (greater than 25K micromho)

1-2 Accessory Equipment Required (continued)

C. Oscillators, Amplifiers, and Signal Sources (cont)

1. CW operation with low power 100-PA-series plug-ins. (cont)

an external power amplifier is required in addition to the oscillator. The oscillator-power amplifier combination must have less than 0.5% distortion. Connect the power amplifier output to EXT. AMPL. INPUT jacks on the 202-PAR-2501. Disconnect the jumper between EF OUTPUT and EXT. AMPL. INPUT jacks, also short the OSC. INPUT jacks.

2. CW operation with high power 100-PA-series plug-ins.

Refer to the power adapter instruction manual for equipment required substituting the Model 202 for the 100B or 100C indicated in the instructions.

3. Tone burst operation with low power 100-PA-series plug-ins.

Refer to para. 1 above for general oscillator and amplifier considerations. In addition, a modulator or tone burst generator is required for generating the gated signal. A variable repitition rate of 10 ms to about 1 sec is typically required, the pulse width being variable to allow a 5% to 30% duty cycle. A 5 volt pulse or gate is required for syncronization of the Vector Component Computer. The Vector Component Computer trigger input is ungrounded (input transformer) with approximately 3K input impedance. The Vector Component Computer has an internal generator for delaying the sample period until after the turn-on transients have disappeared. Syncronization of the turn-on and turn-off of the tone burst is required. Syncronization on signal zero crossings is generally used. Noise, switching transients, D.C. switching components, pedestals, etc., produced by the pulser or modulator must be less than 1% of the peak output. Distortion within the pulse or modulator must be limited to less than 0.5%.

1-2 Accessory Equipment Required (continued)

C. Oscillators, Amplifiers, and Signal Sources (cont)

4. Pulse operation with high power 100-PA-series plug-ins.

Paragraphs 2 and 3 above apply as well to high high power measurements. In addition the Servo Control Unit must be capable of operation with pulsed signals. A SERVO SAMPLER is required to allow use of the Dranetz SERVO CONTROL UNIT Model 501 in pulsed operation. This is connected between the COMP Terminals of the HIGH POWER ADAPTER and the SENS input terminals of the SERVO CONTROL UNIT (501). A Sampling Voltmeter Model 215 is used as the servo sampler.

5. Operation with 202-PA-series plug-ins.

(See the plug-in instruction manual)

1-3 Accessories Supplied

Plug-ins and adapters are not supplied with the Vector Component Computer, but are available separately as required. 100-PA series and 202-PA series plug-ins for various functions are described in the attached brochure.

A. Three wire power cord.

B. Mating Connectors.

1. One Amphenol (AUX. EQUIP) mating connector (26-4301-16S)

2. Three Cannon XLR4-11C mates with DC output connectors and Scope Z-Axis connector

3. One Cannon XLR3-11C mates with REC. CONTROL connector

4. One Cannon XLR5-11C mates with AC output connector.

C. Two extenders for trouble shooting.

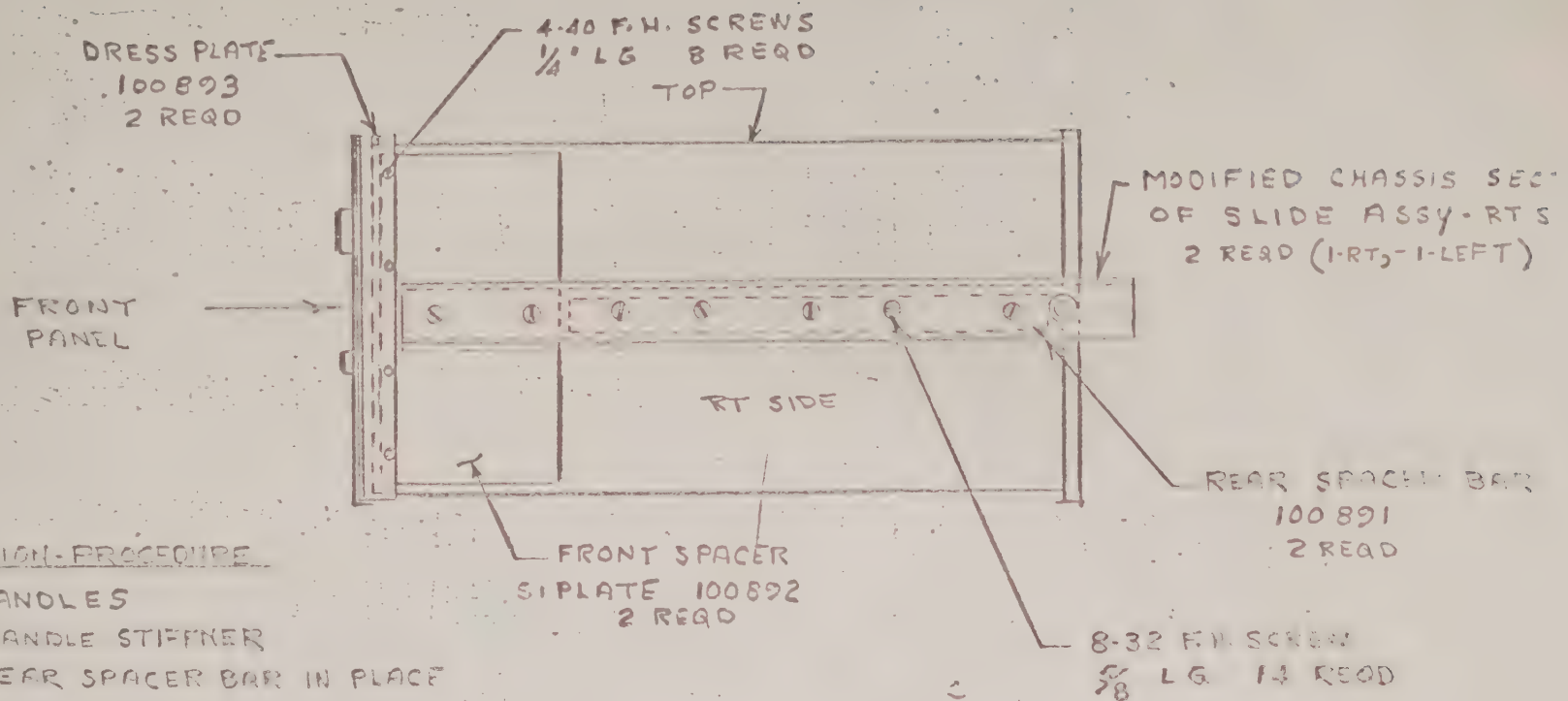
Optional items include:

D. Bridging Unit 100, 713B for use with 100-PA-series plug-ins. (optional)

E. Emitter Follower Rear panel plug-in 202-PAR-2501 for use with 100-PA-series low power plug-ins. (optional)

INSTALLATION PROCEDURE

FOR RACK MOUNTING



INSTALLATION-PROCEDURE

1- REMOVE HANDLES
2- REMOVE HANDLE STIFFNER
3- PLACE REAR SPACER BAR IN PLACE
4- PLACE FRONT SPACER PLATE IN PLACE
5- MOUNT MODIFIED CHASSIS SECTION OF SLIDE ASSEMBLY OVER FRONT SPACER & REAR SPACER USING 8-32 F.H. SCREW 5/8 LG. 14 PCS
6- MOUNT DRESS PLATE USING 4-40 F.H. SCREWS 1/4" LG 8 PCS

Table 1 (continued)

FIG. 1 INDEX NO.	NOMENCLATURE	FUNCTION
3	GO light	Green light, on only after a complete and correct cycle of operation. Indicates that the sample and hold circuitry has sampled the computer outputs. Off when the reference is less than 2.1V rms (5.9V p-p) in any position of the function switch. Off in the vector component position of the Function switch when the signal frequency is lower than the frequency selected by the Frequency Range switch. Off in the Vector Magnitude position of the Function switch when the signal input is less than 10% of full scale. (202 only) Off when the signal frequency is too low for the sample time selected. Note that a delay has been added to the "ON" indication which prevents the light from blinking during the fast sampling rates, however, the light blinks during the longer sampling rates, this is normal.

Table I (continuted)

FIG. 1 INDEX NO.	NOMENCLATURE	FUNCTION
4	OUT OF LIMITS light	Red light. Off under normal operation. On when the reference signal exceeds 3.9V rms (11 V p-p) during the sample time. On when the information signal exceeds 150% of full scale during the sample time. On when the signal frequency is too low for the sample time selected. On when the computing element outputs are overloaded for any reason. An audible alarm controlled by a rear panel switch is also provided.
5	SAMPLE DELAY FINE control R101	Varies the sample delay within the range selected by the RANGE control (6).
6	SAMPLE DELAY RANGE switch SW 101	Varies the sample delay in steps. Note that this circuit operates in both CW and PULSE operation. In CW operation the switch must be turned fully CCW to the shortest SAMPLE DELAY TIME position.
7	F.S. BAL control R102 (Model 202 only)	A screw driver control which varies the gain of the quadrature channel independently in the VECTOR MAGNITUDE position of the FUNCTION switch. The quadrature channel output is proportional to -cos ϕ in this operating mode.

Table I (continued)

FIG. 1 INDEX NO.	NOMENCLATURE	FUNCTION
7A	Zero (Magnitude)	A screw driver control for setting the zero point of the /Z/ D.C. output.
7B	F.S. (Magnitude)	A screw driver control for setting the full scale point of the /Z/ D.C. output.
7C	Zero (Phase)	A screw driver control for setting the zero point of the phase output.
7D	F. S. (Phase) (Model 202A only)	A screw driver control for setting the full scale point of the phase output.
8	FUNCTION switch SW 104 (Model 202A only)	A three position switch. In the "MEASURE" position the unit is in its normal operational mode. In the "CAL. REAL" position, the real component output may be calibrated and the phase zero may be set. In the "CAL. QUAD" position, the quadrature component output may be calibrated and the phase sensitivity may be set at -90 degrees. The /Z/ zero and full scale positions may be set in either "CAL." position.

Table I (continuted)

FIG. 1 INDEX NO.	NOMENCLATURE	FUNCTION
8	FUNCTION switch SW 104 (Model 202 only)	A three position switch. In the "Vector Components" position the Real channel output is proportional to the inphase component of the input signal, the quadrature channel output is proportional to the quadrature component of the input signal. In the CAL position both outputs are proportional to the in-phase component of the input signal. Also the "Frequency Range" switch is inoperative. In the "Vector Magnitude" position the Real channel output is proportional to magnitude (signal amplitude without phase considerations). The "X" channel output is proportional to minus the cosine of the phase angle between information signal and reference signal at low frequencies and for power factors greater than .600. In the Vector Magnitude position the V.C.C. is disabled if the information signal is less than 10% of full scale.
9	FREQUENCY RANGE switch	A five position switch which controls the Quadrature channel frequency range in "Vector Components" position of the "Function" switch. The V.C.C. is disabled if

Table I (continued)

INDEX NO.	NOMENCLATURE	FUNCTION
9	FREQUENCY RANGE switch (continued)	the signal frequency is below the lower limit of the frequency range selected.
10	SAMPLE TIME switch SW 105	An eleven position switch calibrated in milliseconds which selects the nominal sampling time of the V. C. C. The total computing time required by the V. C. C. is always greater than the sample time selected. Additional time is required for starting and stopping of the sampling synchronous with the signal frequency, processing of the sampled data and transferal to the sample and hold circuits. The total computing time required varies between 70% and 170% of the sample time selected depending upon range.
11	F. S. MAG control R 103	A screw driver adjust control which is used for full scale calibration of the V. C. C. with different plug-ins. It varies simultaneously the gain of all channels.
12	REAL ZERO control	A screw driver adjust control which is used to zero the Real channel output.

Table 1 (continued)

FIG. 1 INDEX NO.	NOMENCLATURE	FUNCTION
13	QUAD ZERO control	A screw driver adjust control which is used to zero the quadrature channel output.

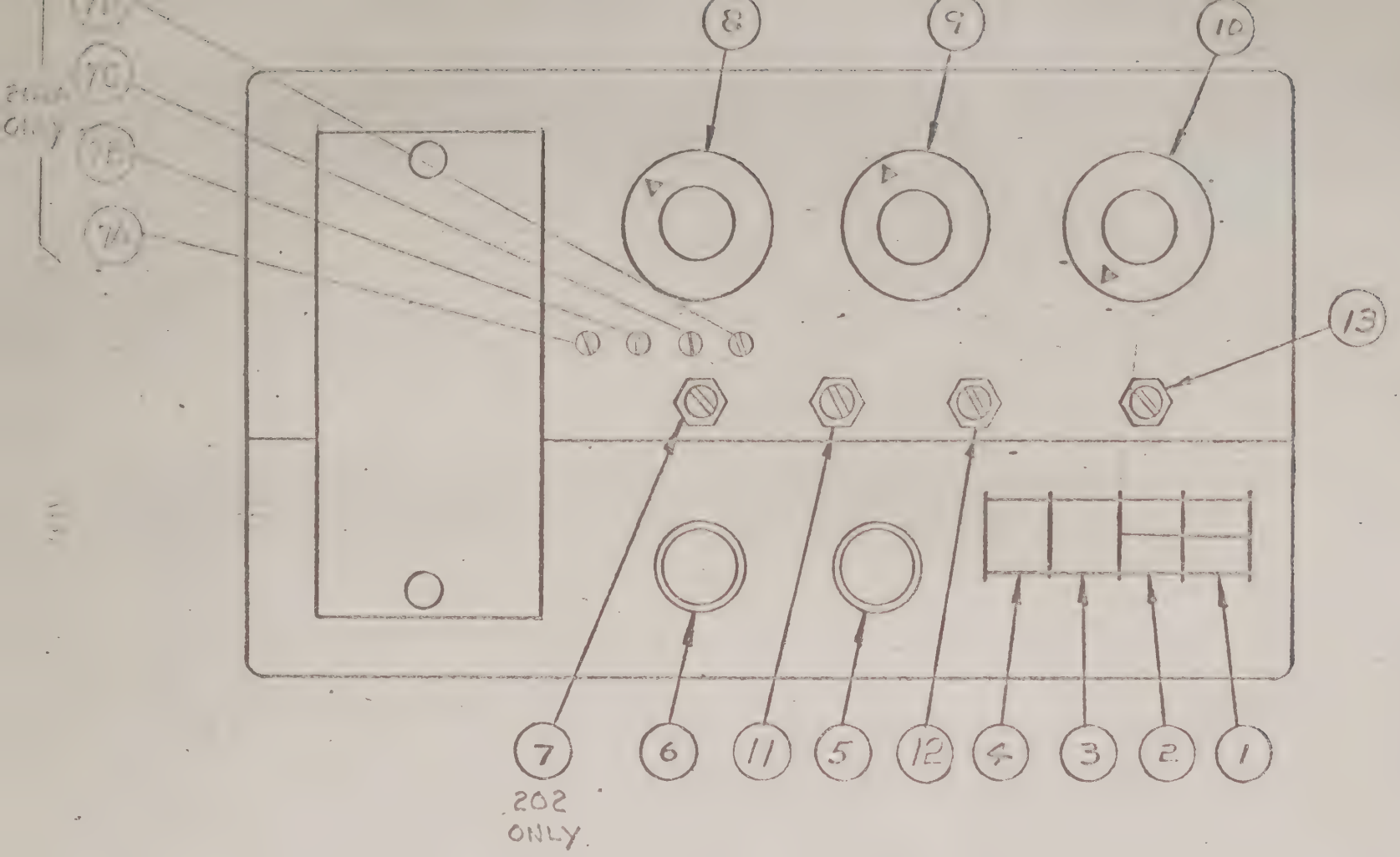


FIGURE I.

Table II-IDENTIFICATION AND FUNCTIONS OF REAR PANEL ADJUSTMENTS, TERMINALS, AND CONNECTORS. Figure II is shown with an Emitter Follower plug-in Model 202-PAR-2501 installed.

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
1	AUX. EQUIP connector J601	A sixteen pin connector which provides various signals and power for any auxiliary equipment which might be used in conjunction with the V.CC The pin functions are:

PIN#	FUNCTION
1	3V AC Meter Grd. Return
2	Grd. Return
3	Internal Trigger Output
4	Grd. Return
5	Ref. Level Indicator Output
6	DC Output Ground Return
7	Real Ch. DC Output
8	MARK signal Output
9	Aux. Power Ground
10	3V AC Meter Output
11	Grd. Return
12	+36V Aux. Power
13	-36V Aux. Power
14	Grd. Return
15	Quad. ch DC Output
16	RESET Signal Output

Table II (continued)

INDEX NO.	NOMENCLATURE	FUNCTION
2	D.C. OUTPUT connector J602	A four pin connector which allows connection to external readout devices. The pin functions are Pin# 1: Real ch DC OUTPUT Pin# 2: GROUND RETURN Pin# 3: Quad ch DC OUTPUT Pin# 4: "Ø" Output (Phase output see 4 below)
3	D.C. OUTPUT connector J603	A four pin connector which allows connection to external readout devices. The pin functions are: Pin# 1: Real ch DC Output Pin# 2: GROUND RETURN Pin# 3: Quad ch DC Output Pin# 4: "Z" output signal (see 4 below) (Magnitude output)
4	A.C. OUTPUT connector J604	A five pin connector for oscilloscope monitoring of information and reference signals. Both are scaled to approximately 3 V p-p Both have a pedestal which corresponds to the total computing time of the V.C.C. thus allowing the operator to adjust the sample delay during pulse operations. On equipment which has the Z-Ø converter the "Z" magnitude and Ø phase reference signals are

Table II (continued)

INDEX NO.	NOMENCLATURE	FUNCTION
4	A.C. OUTPUT connector J 604 (continued)	available at pins 4 & 5 and also pins 4 of the DC output connectors (item 2 & 3 above). The pin functions are:

Pin #	Function
1	Information Signal Output
2	Grd. Return
3	Reference Signal Output
4	"Z" Magnitude Output
5	"ϕ" Output

INDEX NO.	NOMENCLATURE	FUNCTION
5	SCOPE Z AXIS connector J605	A four pin connector for oscilloscope Z AXIS control, and syncronization. The "RESET" signal can be used for oscilloscope blanking, the "MARK" for intensification, and the TRIGGER for syncronization The trigger is also available at the TRIGGER OUTPUT connector.

Pin #	Function
1	"MARK" output
2	GROUND
3	"RESET" output
4	"TRIGGER" output

Table II (continued)

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
6	REC. CONTROL connector J606	A three pin connector providing control output for X-Y recorders or Digital Voltmeters. The "seek" output, a -1 milliamp pulse, corresponds to the completion of the compute operation of the V.CC. This pulse is suitable for "unmuting" of X-Y recorders or for the "read" command of digital voltmeters. The "disable" output, a -1 milliamp signal is present whenever the OUT OF LIMITS light is "ON". This signal may be used for "Pen lift" on X-Y recorders.
7	RESET control R604	A screw drive r control for adjusting the "voltage" amplitude of the "RESET" output. A -1 milliamp signal is generated. The "RESET" control is a 25K reostat connected across this current source. By varying the resistance of the reostat from 0 to 25 K, the output "voltage" varies from 0 to -25V.
8	COMP. LEVEL control R605	A screw driver adjustment of the comparator level. Normally, a maintenance adjustment which adjusts the full scale outputs to 5 volts DC with the front panel. F.S. Mag Control Centered.

Table II (continued)

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
9	MARK control R603	A screw driver control for adjusting the "voltage" amplitude of the "MARK" output. A +1 milliamp pulse is generated during the operation of the V.C.C. The control operates similarly to 7 above.
10	FUSE 1/2 A.-MDL F602	1/2 AMP slow-blow fuse, type 3 AG-MDL, for protection of the signal circuits power supply in the V.C.C.
11	FUSE 1/4 A F 601	1/4 AMP type 3AG fuse for protection of the fan.
12	117V 60 Hz receptacle J607	The power input receptacle. A mating power cord is supplied. POWER GRD is isolated from the V.C.C. case and circuit grounds. The center pin of the receptacle is the third wire of the power cord. The third wire, case ground, and circuit ground are brought into the front panel plug-in. The case ground and circuit ground are tied together within the plug-ins. If it is necessary to connect the third wire also this must be done within the plug-in.

Table II (continued)

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
13	FUSE 1A S.B. F603	1 Amp slow-blow fuse type 3AG for protection of the plug-in power supply.
14	DELETED	
15	SPARE binding posts	
16	HUM INPUT jacks J609	Binding posts. During extremely high conditions of 60 cycle pickup or other sources of noise it may be necessary to inject a signal via the HUM INPUT jacks to cancel the noise.
17	TRIGGER OUT comector J610	Binding posts. A 10V positive pulse from the sample delay timer the leading edge corresponds to the trigger input, the trailing edge to the end of the sample delay (used for scope sync).
18 and 19	TRIGGER INPUT connectors and Trigger level control J611 & R602	Binding posts. An input for syncronizing the V.C.C. with the pulser or modulator during PULSE operation. A 5V pulse or square wave is required. Both terminals are floating (transformer input). The red terminal must be positive going with respect to the black. The trigger level control is a variable attenuator allowing input levels to 25V peak.

Table II (continued)

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
20	AUDIO ON switch SW601	Toggle switch which connects buzzer to the OUT OF LIMITS lights to provide an audible alarm during overloads. The audible alarm is useful in system setups where the operators attention may be on some other phase of the operation.
21	BLOWER M601	A fan for cooling. The filter may be cleaned by rinsing in water.
22	E.R. OUTPUT jack	A red binding post. The output of a power emitter follower in the 202-PAR-2501. Used as the signal source for 100-PA-series low power plug-ins. Normally connected to the EXT. AMPL. INPUT terminal except when the test sample is greater than 25 K micromhos (less than 40Ω) in which case an external amplifier is required.
23	EXT. AMPL. INPUT jack	A red binding post. This terminal is connected directly to the front panel plug-in. The reference signal is provided through this connection to the 100-PA-series low power plug-ins. Normally connected to the EF OUTPUT terminal except when the test sample is greater than 25K micromhos (less than 40Ω) in which case an external amplifier is required.

Table II (continued)

FIG. II INDEX NO.	NOMENCLATURE	FUNCTION
24 and 25	GROUND jacks	Black binding post. The ground return for osc. and EXT ampl.
26	OSC. INPUT jack	A red binding post for the oscillator which drives the emitter follower in the 202-PAR-2501.

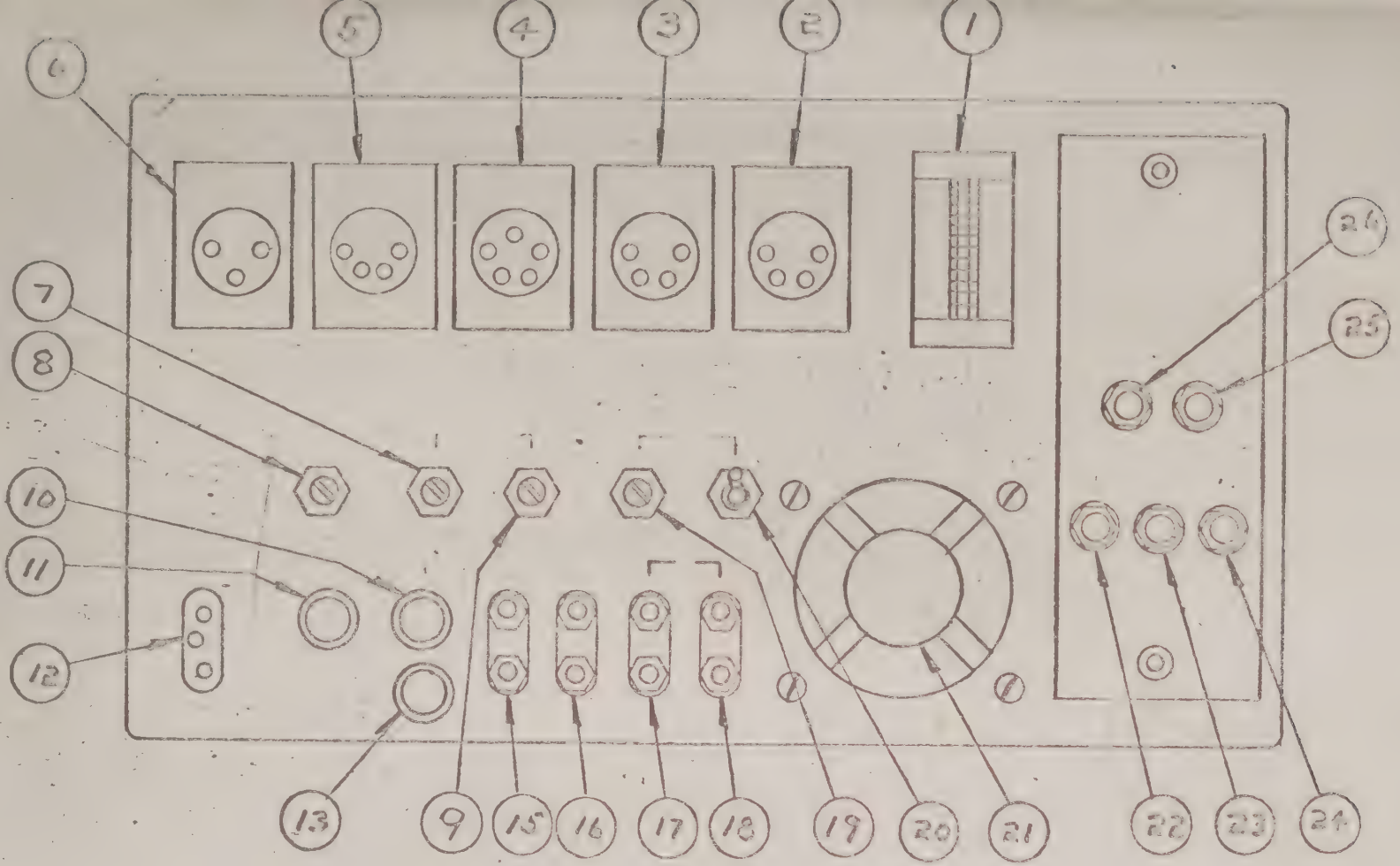


FIGURE 2L

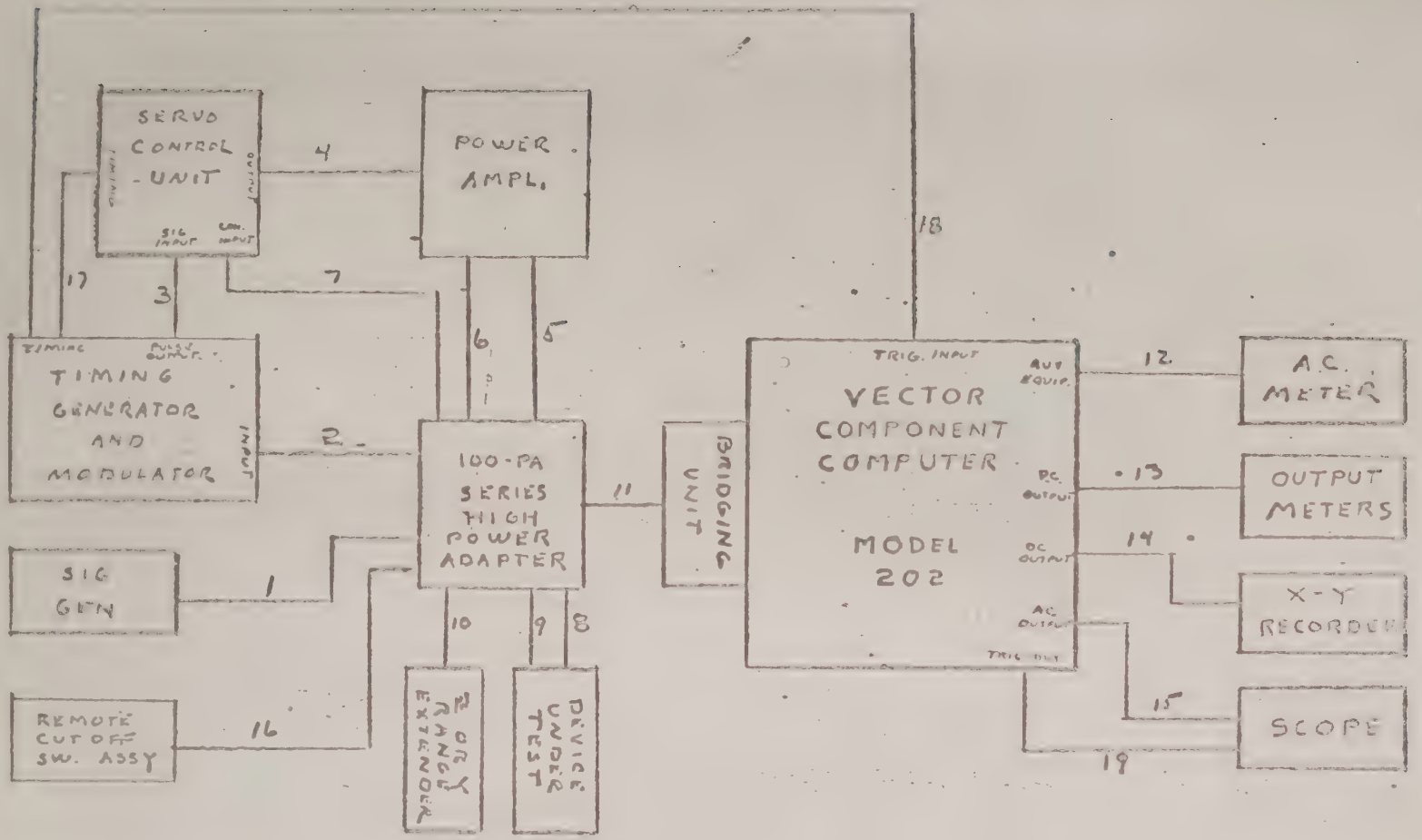


FIGURE III

SYSTEM INTERCONNECTIONS FOR HIGH POWER IMPEDANCE/ADMITTANCE

2-2 SYSTEM INTERCONNECTIONS

A. CW Measurements

Using the bridging unit connect the impedance or admittance plug-in to the Vector Component Computer. Refer to FIG. III. Connect the VTVM, output meters, X-Y recorder and oscilloscope to the Vector Component Computer. If a high power adapter is used, refer to it's instruction manual for additional interconnection information, substituting the Model 202 for the 100B or 100C indicated therein.

B. PULSED Measurements with High Power Adapters.

1. Connect the system as indicated in Figure III and Table III.

2. Before turning the equipment on inspect all ground connections. The Ground Block J5 on the High Power Adapter must be the common ground point for the system.

Table III CABLES AND CONNECTION INFORMATION

FIG III Cable No.	DESCRIPTION AND REMARKS
1	Connect a shielded cable from the signal generator to the FROM SIG. GEN. terminals on the adapter. NOTE: If multiple grounds will result a 1:1 isolation transformer is supplied with the adapter.
2	Connect shielded cable from the TO PWR AMPL terminals on the adapter to the signal input terminals on the modulator. Note that for simplification the Timing Generator and Modulator are shown as one unit.
3	Connect a shielded cable from the pulsed output of the modulator to the signal input of the Servo Control Unit.

Table III (continued)

FIG III Cable No.	DESCRIPTION AND REMARKS
4	Connect a shielded cable from the signal output terminals of the Servo Control Unit to the Power Amplifier input terminals. NOTE: It may be necessary to connect a pre-amplifier and band pass filter at this point.
5	A coaxial cable rated at 6 KV rms connects the power amplifier output to the adapter.
6	A 30 ampere capacity wire is needed for the ground return between power amplifier output and GROUND BLOCK J5 on the adapter.
7	Connect a shielded cable from the COMP. output of the adapter to the control input of the SERVO Control Unit.
8	A coaxial cable rated at 6Kv rms connects J2 of the adapter to the device under test.
9	A 30 ampere capacity wire as short as practical is needed for the ground return between the device under test and GROUND BLOCK J5 on the adapter.
10	Z or Y range extender connections, refer to the adapter instruction manual.
11	The plug-in assembly which interconnects the adapter and the bridging unit.
12	A shielded cable from AUX. EQUIP. connector on the V.C.C. to the AC meter. See Table II for pin connections.
13	A multi wire cable connecting the output monitoring meters to either the DC OUTPUT connectors or the AUX. EQUIP. connector on the V.C.C. See Table II for pin connections.

Table III (continued)

FIG III Cable No.	DESCRIPTION AND REMARKS
14	A four wire cable connecting the X-Y Recorder to the DC OUTPUT connector on the V.C.C. If a null detector type recorder, a point plot recorder, or a recorder with remote pen lift is used, and additional three wire cable is needed to connect the REC. CONTROL outputs of the V.C.C. to the appropriate terminals on the recorder. See Table II for pin connections.
15	A pair of shielded cables connecting the oscilloscope inputs to the AC OUTPUT connector on the V.C.C. See Table II for pin connections.
16	The remote cut off assembly supplied with the adapter.
17	A shielded cable connecting the timing input of the Servo Control Unit to an appropriate timing signal from the modulator.
18	A shielded cable connecting the TRIGGER INPUT of the V.C.C. to an appropriate timing signal from the modulator.
19	A shielded cable connecting the TRIGGER OUTPUT of the V.C.C. to the external sync. input of the oscilloscope. If blanking or intensification of the oscilloscope is used, additional shielded cables are required. (See Table II).

2-3 OPERATION

A. General

The Vector Component Computer always operates in a pulsed mode whether the signals applied are CW or pulsed. If the inputs are pulsed an externally applied trigger is required to syncronize the Vector Component Computer with the pulsed signals. If the signals are CW, an internal repetition rate generator is used to trigger the Vector Component Computer. A push button switch and indicator on the front panel allow selection of the desired mode of operation. When the yellow CW light is on the external trigger is prevented from starting the Vector Component Computer. When the blue PULSE light is on the internal repetition rate generator is disabled.

2-3 OPERATION (continued)
A. General (continued)

An internal SAMPLE DELAY timer with a RANGE and FINE control on the front panel allow delaying the start of the Vector Component Computer compute cycle until any transients in the input signals have disappeared. This timer always operates, therefore in CW operation, the SAMPLE DELAY must always be adjusted to the minimum delay (both controls full CCW) to prevent random operation.

The SAMPLE TIME control on the front panel selects the nominal time the Vector Component Computer requires for data acquisition. In normal operation the sample time must be adjusted to provide a minimum of 8 full cycles of signal. For instance, if the lowest frequency to be measured is 800 Hz (a 1.25 ms period), 8 times 1.25 ms or 10 ms is the minimum sampling time that can be used. If some loss of accuracy is acceptable, computation can be performed on as few as three cycles of signal; however this is not recommended because the Vector Component Computer may not operate on every trigger signal.

The total computing time required by the Vector Component Computer is always somewhat different than the sample time selected by the SAMPLE TIME control on the front panel. This is because a number of internal functions are performed in addition to the actual acquisition of the data. The total computing time required varies from 70 to 170 percent of the sample time selected depending upon the signal frequency and the relative amplitude of the input signals.

A simplified description of a complete cycle of operation will assist the operator in using the Vector Component Computer. Refer to the waveforms and timing diagram of Figure IV. The cycle is initiated by a trigger pulse (A). This may be internally generated or supplied by the modulator at the instant that the pulsed signal is initiated. FIG. IV (B) shows the gated reference signal. Both the amplitude and phase of this signal are utilized by the Vector Component Computer in it's computation. FIG IV (C) shows the information signal. The amplitude and phase of this signal are proportional to the impedance or admittance of the device under test, properly scaled by the plug-in or adapter used. The amplitude is also proportional to the reference signal amplitude. For instance, if the reference signal varies 10% from the nominal 3V rms required, the information signal will vary 10%. This would result in a 10% error in the DC outputs; however, the Vector Component Computer computes

2-3 OPERATION (continued)

A. General (continued)

The "Sample Time" is the time required by the Vector Component Computer for acquisition of the data. The nominal value is selected by the SAMPLE TIME control on the front panel. This time also varies since both the start and stop must be syncronized with signal zero crossings.

The "Processing Time" is the final period required by the Vector Component Computer. During this time the data is processed by the Vector Component Computer to become proportional to X or Y without the errors due to reference level variations, harmonic distortion, timing errors, gain errors, etc. At the end of this time period, a signal is generated indicating that the Vector Component Computer has correctly computed or processed the data. This signal returns the MARK signal to zero, switches the sample and hold circuits to the new data values and lights the GO light. Note: that a time delay keeps the GO light on during the faster sampling times; however, with long sampling times, the GO light will blink. This is entirely normal.

The above discussion supposes pulsed signals, in CW operation the trigger pulse (A) is supplied by an internal rep. rate generator and both FIG IV (B) and FIG. IV (C) are CW signals. During CW the sample delay controls must be placed in the minimum delay position, both RANGE and FINE controls CCW.

B. Making Measurements (Model 202 only)

The initial set up prior to actual measurements is identical regardless of the plus-in or adapter used, the measurement to be made (Z or Y) or whether the test is under CW or pulsed conditions. Refer to Section I and the preceeding paragraphs for equipment required and the necessary interconnections. Before applying power to the system, turn all level or gain controls to minimum, place the Vector Component Computer FUNCTION switch to CAL and the MODE switch on the plug-in or adapter to CAL ZERO. Set the sample delay controls for minimum delay.

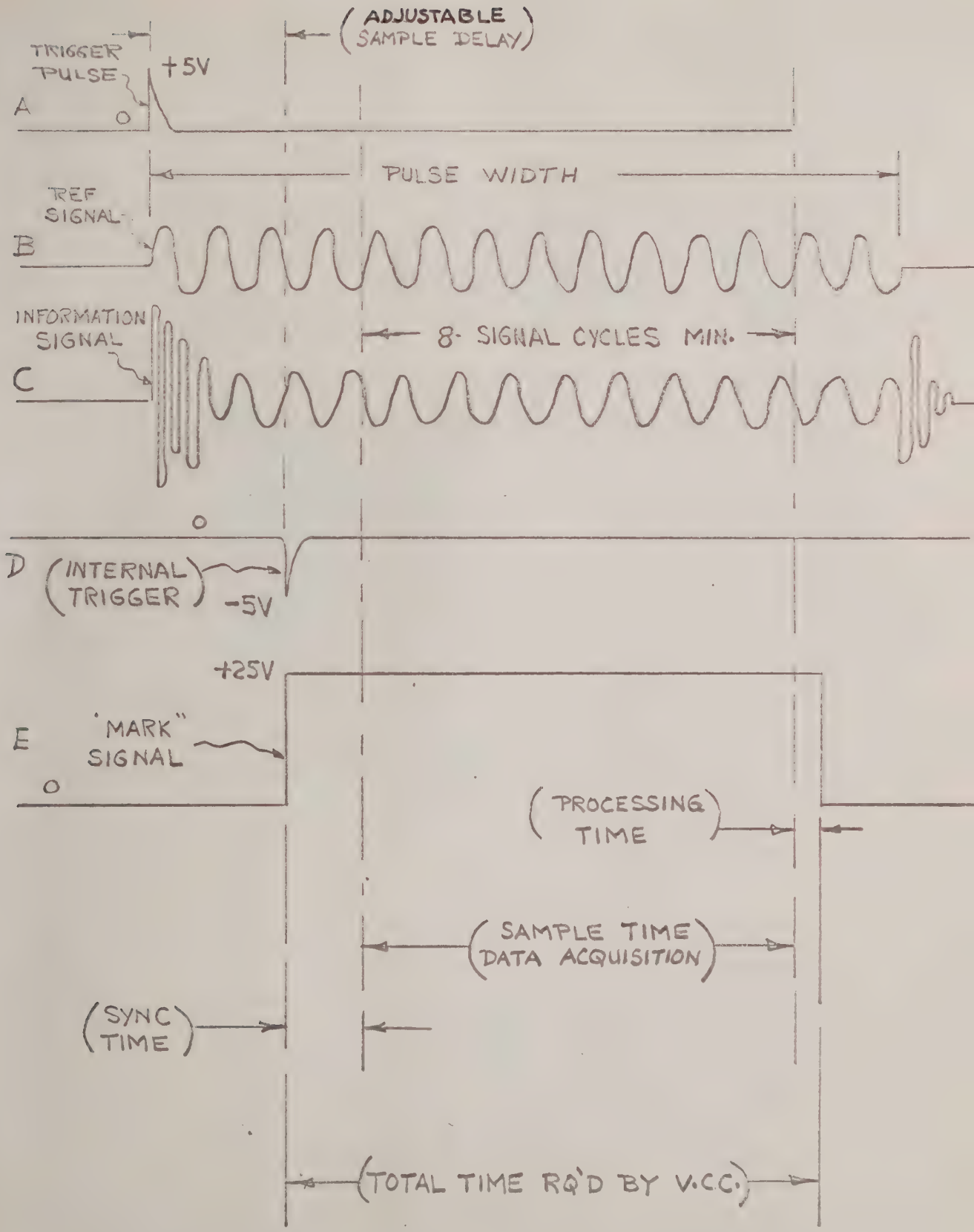


FIGURE IV

TIMING DIAGRAM AND SIGNIFICANT WAVEFORMS

2-3 OPERATION (continued)

B. Making Measurements (continued)

Turn on all equipment and allow the necessary warm-up time. If a Z or Y measurement is being made, adjust the range switch to maximum. Place the Vector Component Computer in CW or PULSE, depending upon the mode of test.

Set the oscillator frequency to the lowest frequency of test. Calculate the time required for 8 cycles. Set the SAMPLE TIME to a time equal to, or larger than, this calculated time. In pulse operation, set the pulse width of the modulator to at least twice the Vector Component Computer sample time. Adjust the modulator repetition rate for the desired duty cycle. Insure that trigger pulses are available to the Vector Component Computer. Adjust the appropriate gain or level controls on the servo, P.A., and adapter such that the AC METER reads 3 V rms for CW operation or the oscilloscope indicates a 3 V p-p reference signal. Approximately one minute is required for the Vector Component Computer to clear itself of the overloads that occured when power was applied. In pulsed operation, adjust the sample delay so that the MARK signal appears centered on the reference signal. The GO light should be "ON". Adjust the output meter zero and the X-Y recorder zero. Place the MODE switch on the plug-in or adapter to CAL F. S. . If the output meters have sensitivity controls, adjust these for "Full Scale". If not, adjust the F.S. MAG control on the Vector Component Computer.

Also adjust the X-Y recorder full scale. The Vector Component Computer is now calibrated, this need not be done again unless the plus-in or adapter is changed. The X-Y recorder will require recalibration if the paper is changed.

Place the FUNCTION switch on the Vector Component Computer in "Vector Magnitude". Place the MODE switch on the plus-in or adapter to MEASURE. In pulse operation observe the reference and information signals on the oscilloscope. If transients are present, readjust the sample delay. Sweep through the frequency range monitoring the "R" channel output and the pulsed wave forms. Adjust the Z or Y RANGE controls on the plug-in or adapter such that the madimum "R" channel output is less than Full Scale. Place the FREQ. RANGE switch on the Vector Component Computer in a position that encompasses the frequency range of test. Place the FUNCTION switch on the Vector Component Computer in Vector Components.

C. Making Measurement (Model 202A only)

The initial set up prior to actual measurements is identical regardless of the plug-in or adapter used, the measurement to be made (Z or Y) or whether the test is under CW or pulsed conditions. Refer to Section I and the preceeding paragraphs for equipment required and the necessary interconnections. Before applying power to the system, turn all level or gain controls to minimum, place the Vector Component Computer FUNCTION switch to CAL REAL and the MODE switch on the plug-in or adapter to CAL ZERO. Set the sample delay controls for minimum delay.

Turn on all equipment and allow the necessary warm-up time. If a Z or Y measurement is being made, adjust the range switch to maximum. Place the Vector Component Computer in CW or PULSE, depending upon the mode of test.

Set the oscillator frequency to the lowest frequency of test. Calculate the time required for 8 cycles. Set the SAMPLE TIME to a time equal to, or larger than, this calculated time. In pulse operation, set the pulse width of the modulator to at least twice the Vector Component Computer sample time. Adjust the modulator repetition rate for the desired duty cycle. Insure that trigger pulses are available to the Vector Component Computer. Adjust the appropriate gain or level controls on the servo, P.A., and adapter such that the AC METER reads 3 V rms for CW operation or the oscilloscope indicates a 3 V p-p reference signal. Approximately one minute is required for the Vector Component Computer to clear itself of the overloads that occurred when power was applied. In pulsed operation, adjust the sample delay so that the MARK signal appears centered on the reference signal. The GO light should be "ON".

Place the MODE switch on the plug-in or adapter to "CAL. ZERO". Set R channel zero for zero V DC on the R channel DC output. Set the plug-in "MODE" switch to "CAL. F.S.". Set the "F.S. MAG." control for full output from the R channel DC output (5.00 V DC). Set the "MAGNITUDE F.S." Pot. for full output fromthe /Z/ DC output (1.00 V DC behind 1000 Ω). Set the "PHASE ZERO" Pot. for zero V DC on the PHASE DC output. Return the plug-in "MODE" switch to the "CAL. ZERO" position and set the "FUNCTION" switch to "CAL. QUAD." Adjust the "QUAD. ZERO" control for zero V DC on the quadrature DC output. Return the plug-in "MODE" switch to the "CAL. F.S." position and set the " PHASE F.S." Pot. for a -90° indication (-0.90 V DC behind 1000Ω) on the PHASE DC output.

C. Making Measurement (continued)

Place the FUNCTION switch on the Vector Component Computer in "MEASURE". Place the MODE switch on the plug-in or adapter to MEASURE. In pulse operation observe the reference and information signals on the oscilloscope. If transients are present readjust the sample delay. Sweep through the frequency range monitoring the "R" channel output and the pulsed wave forms. Adjust the Z or Y RANGE controls on the plug-in or adapter such that the maximum "R" channel output is less than Full Scale. Pulse the FREQ. RANGE switch on the Vector Component Computer in a position that encompasses the frequency range of test. Place the FUNCTION switch on the Vector Component Computer in Vector Components.

The system is now ready to plot the data.

SECTION III

THEORY OF OPERATION

3-1 INTRODUCTION

The basic function of the VECTOR COMPONENT COMPUTER is to measure the real and quadrature components of a zero to 30 millivolt information signal using a nominal 3 volt reference signal for phase and amplitude reference. The measurements are made on a sampling basis which provides a measurement capability for rapidly varying or tone burst signals. Since most measurements requiring determination of vector components are in the form of impedance, admittance or transfer functions where the information signal magnitude has a direct relation to the reference signal magnitude, the measurements made have the general form:

A) $$E_{\text{output (real)}} = \frac{V \text{ information}}{V \text{ reference}} \cos \phi$$

B) $$E_{\text{output (quadrature)}} = \frac{V \text{ information}}{V \text{ reference}} \sin \phi$$

Where ϕ is the phase angle between the reference and information signals.

The Model 202 performs the above measurement in the Vector Components mode of operation. In it's Vector Magnitude mode the REAL channel output is:

C) $$E_{\text{output (real channel)}} = \frac{V \text{ information}}{V \text{ reference}}$$

and the QUAD channel output is:

D) $$E_{\text{output (quad. channel)}} = -\cos \phi$$

The Model 202A in addition to outputs A and B above provides output C (Z output) and the phase angle (ϕ output) simultaneously.

In the following paragraphs the theory of operation of the different sections of the quipment are discussed. The most complex section is the computer element boards, which perform three separate and distinct functions. Since each is somewhat complex in itself they are described separately in sections 3-2, 3-3, and 3-4. Section 3-5 discusses the method used to provide multiple sample times.

3-1 INTRODUCTION (continued)

The operation of the basic equipment is described in Section 3-6 excluding special circuits which are separately covered in Section 3-7.

Section 3-8 is devoted to the circuits added for the Model 202A.

3-2 BASIC SYNCHRONOUS DETECTION

A basic half wave synchronous detector is shown in figure VII-a. The reference signal (A) through the OVERDRIVEN AMPLIFIER causes the switch (SW) to toggle between the information signal (C) and ground. When the reference signal is positive the switch is in position 1, when negative, in position 2.

As shown in figure VII-c for an information signal in phase with the reference signal the output at point (D) appears as a half wave rectified waveform. As the relative phase varies through 45° to 90°, as shown in figure VII-d and VII-e, the average value of the waveform at (D) decreases from a positive maximum for in phase signals (0° phase shift) to an average value of zero for a 90° phase difference. As shown in figure VII-f the average value is maximum negative at 180° phase difference.

Vote that full wave rectification can be obtained by connecting switch terminal 2 to the information signal inverted in phase (180° phase inversion).

The function of the synchronous detector can be expressed by the mathematical relation;

V output (average value) = (V information) X (cosine ϕ)

Where ϕ is the phase angle between information and reference signals.

By shifting the phase of the reference signal through a 90° phase shift network the relation becomes;

V output (average value) = (V information) X (sine ϕ)

Thus by using two synchronous detectors and a 90° phase shift, two simultaneous outputs can be provided, one proportional to the real (cosine function) and one proportional to the quadrature (sine function) components of an information signal input of variable phase and amplitude.

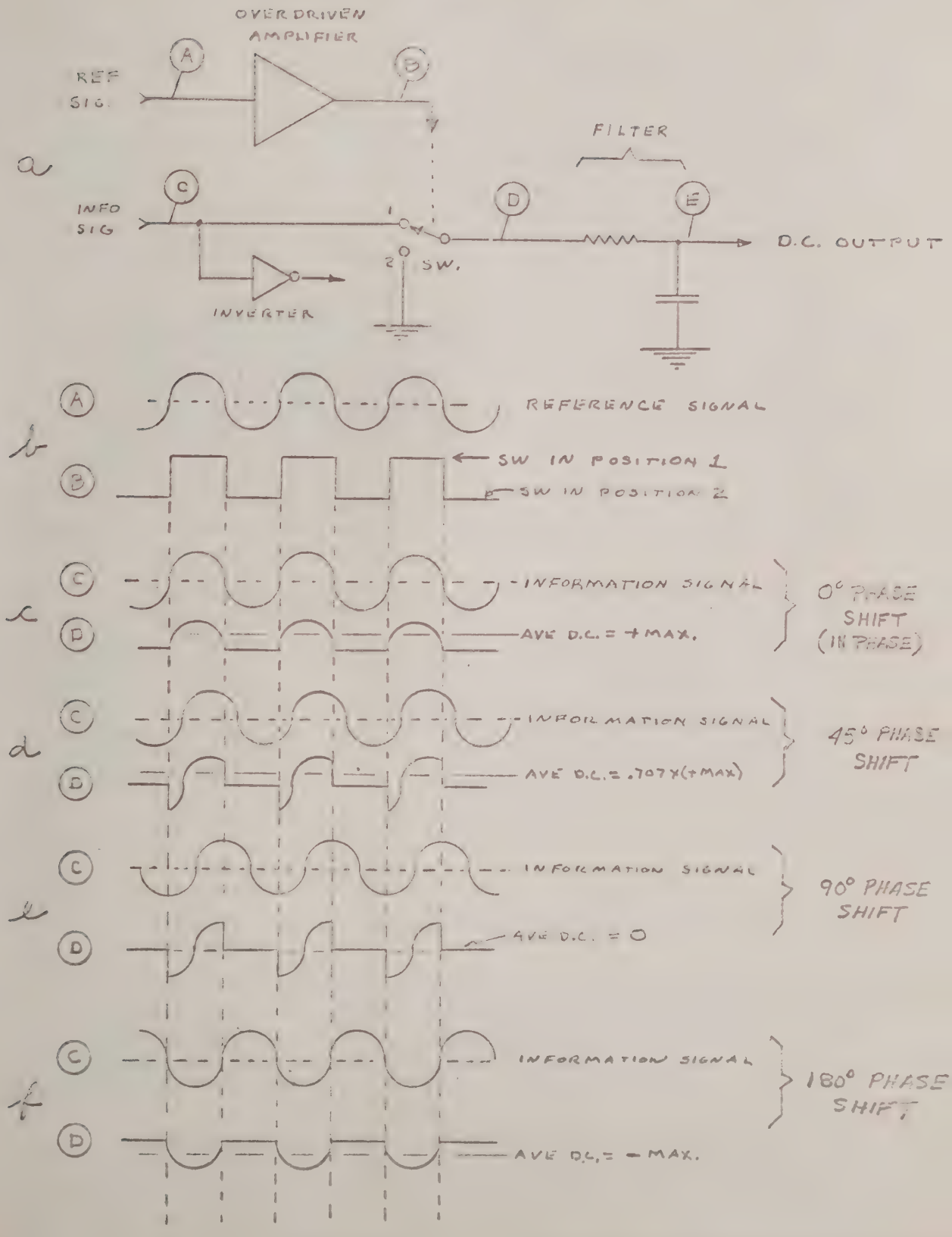


FIGURE VII SYNCHRONOUS DETECTOR

3-3 BASICS OF INTEGRATING TYPE DIVIDER CIRCUITS

An integrating type divider operates in a variable pulse width mode, the pulse width being determined by the divisor signal. Figure VIII shows a typical circuit arrangement. Two identical integrators are used, each composed of a precision resistor, a stable capacitor, and a high gain operational amplifier. Assume both integrators are initially reset to zero output, this can be accomplished by shorting across the capacitors with a switch.

The sequence of operation is initiated by a trigger pulse (A). The trigger sets the flip-flop output (D) to the high state causing switches SW1A and SW1B to move to position 1. If V REF is + 5.00 Volts DC the signal at point (C) will reach +5.00 Volts in a time interval determined by the time constant of R1B and C1B, at which time the output of the comparator (E) changes to the high state, resetting the flip-flops. This causes SW1A and SW1B to move to position 2 which stops the integration.

When V REF increases, the signal at (C) reaches + 5.00 volts in a shorter time interval, when it decreases a longer time is required.

Now if the signal channel obtains it's input signal from a voltage divider composed of resistors R_s and R_x (R_s is approximately 100 times R_x) and a gain of -100 is used, the signal levels in both channels will be the same. With V REF set to + 5.00 volts, Vx will be + 0.05 volts. The time constant of R1A C1A can be adjusted for precisely + 5.0 Volts at V output (D). Now if V REF is increased to + 6.0 volts, V_x will be + 0.06 volts, however V output (D) will still be + 5.00 volts at the end of the integrating time because this time has decreased in proportion to the increase in V REF.

The function performed by the circuit is:

$$V_{output} = \frac{-Vx\ (100)}{-V\ REF} K_1$$

K_1 is a function of the initial integrating time and is 5.00 for the example shown.

With R_s equal to 100 times R_x, variations in R_x will have practically no effect on the current through R_s (and R_x) therefore, I_s which is the same as I_x, is proportional to V REF. The function performed by the voltage divides network and the intergrating type divider in combination is;

3-3 BASICS OF INTEGRATING TYPE DIVIDER CIRCUITS (cont)

$$V_{output} = \frac{-V_x (100)}{-V_{REF}} K_1$$

$I_x \approx V_{REF}$ ($\approx$) = Proportional to

$$V_{output} = \frac{V_x (100)}{I_x} K_1$$

$$V_{output} \approx \frac{V_x}{I_x} K_z \qquad K_z = 100 K_1$$

Since Vx is equal to Ix Rx, the above may be written us:

$$V_{output} \approx \frac{I_x R_x}{I_x} K_z = R_x K_z$$

The output voltage is proportional to Rx.

This is the principle of operation of many resistance measuring devices because it provides a linear scale rather than the cramped scale of the typical multimeter type, also by using the divider the output is independant of the reference voltage. Note: also that until frequency response and/ or switching time become significant the integrating time (sample time) can be very fast, easily less than a millisecond with solid state switches. By using AC signals for V REF, AC impedance ($\not{Z}x$) may be measured. (A rectifier is needed in each channel for AC)

By swapping the inputs to SW1A and SW1B at pins #1 another useful function results;

$$V_{output} \propto \frac{I_x}{V_x} K_z \qquad R_x = \frac{V_x}{I_x}$$

$$V_{output} \propto \frac{I}{R_x} K_z \approx G_x K_z$$

Where Gx is the conductance. Again using AC signals, Admittance (Yx) is the result.

Similarily the voltage divider can be replaced with a 3 or 4 terminal "black box", and (with AC signals) the transfer function or frequency response may be measured.

A disadvantage of significance is that the signal to the reference channel cannot approach zero and in most cases is limited to relatively small variations around the designed nominal input level . $\pm$ 30% variations are the extreme limits for this equipment.

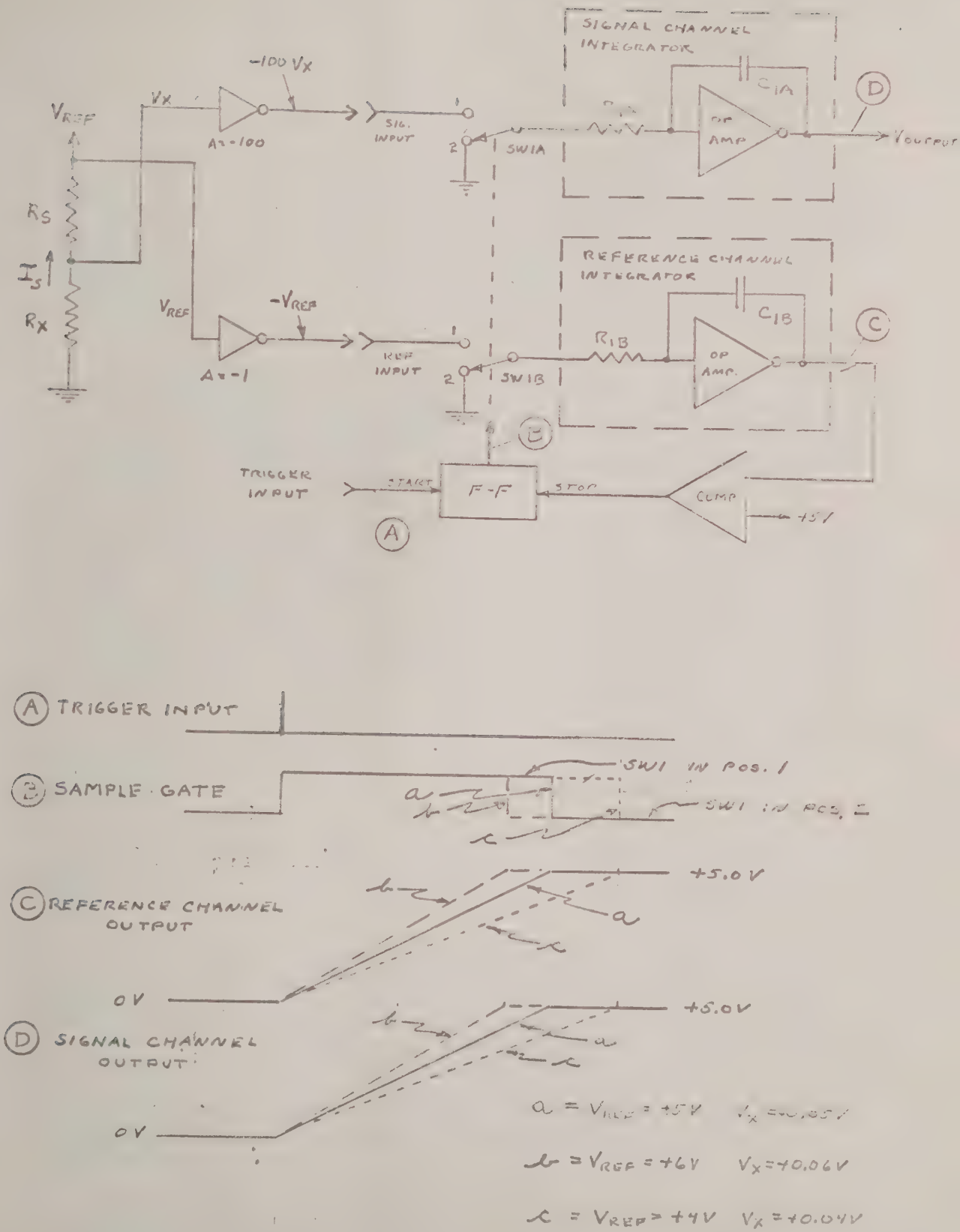


FIGURE VIII INTEGRATING DIVIDER

3-4 BASICS OF SAMPLING DETECTORS

A full-wave rectifier and a low pass filter combine to make the typical AC Detector. Under steady state conditions the D.C. output is proportional to the average value of the AC input. The step response of a typical low pass filter , however, is relatively slow since it is usually necessary to use a long time constant to reduce the ripple at the output. A gated integrator can replace the low pass filter for fast measurements. It's output is D.C. at the end of the sampling or integrating time, however, a minor difficulty arises.

By definition the average value of an AC waveform must be measured over an integral number of cycles of the waveform, 1, 2, 3, 4, etc. An integrator with a finite integrating time would provide the exact average value of an AC waveform only for those frequencies whose period was a multiple of the integrating time. For all other frequencies there would be an error.

By synchronizing the start and stop of the integration (sample) time to positive going zero crossings of the signal, the requirement for measuring an integral member of cycles can be met however the magnitude will be in error by the ratio of the actual integrating time (sample time) to the designed nominal integrating time. The use of an additional channel to integrate a known reference signal allows measurement of the error caused by sample time variation and in addition, with some control circuits, provides the means for correcting a signal channel output.

Figure IX shows a simplified diagram of a circuit arrangement for precision AC detection very rapidly. It is similar to the divider circuit discussed previously in section 3-3 with a few additional components.

Assume both the signal input and the reference input have an amplitude of 5 volts (average value). Reset Gate (P) , occuring sometime before the measurement cycle, closes SW 3A and SW 3B, discharging both integrators in readiness for a measurement.

A trigger (G) is applied firing the one shot. The one shot output, the start gate (H) , enables AND 1 which allows the sample gate flip-flop to be set by the next differentiator output pulse (F) . The sample gate (J) when high moves SW1A, SW1B, and SW1C to position 1. Both integrators start integrating as shown in (K) and (L) . Both time constants are identical and provide +5.00 volts output in the designed integrating time. When the reference detector output (L) reaches +5.00 volts the comparator output (compute signal (M)) goes high enabling AND 2 which allows the next differentiator output pulse (F) to shut off the sample gate (J) opening SW1A and SW1B and Closing SW1C.

At this time both integrators (Detectors) have an error proportional to the ratio of the actual sample time (Ts) to the designed integrating time (TI).

3-4 BASICS OF SAMPLING DETECTORS (cont)

By simultaneously discharging both integrators, through SW2A, SW2B, R2A and R2B under control of the compute gate (N), until the reference detector reaches +5.00 volts, the error due to the variation in sample time is corrected. Since the measurement was made for an integral number of signal cycles, three in this case, the DC signal output is the true average value of the AC signal input. In addition if the information signal and reference signal are related as discussed in section 3-3, this circuit also performs the divider function.

The input-output relationship is;

$$V_{output\ (DC)} = \frac{V_{information\ (AC)}}{V_{reference\ (AC)}}$$

If the full-wave rectifiers are replaced with the synchronous detectors of section 3-2 the vector components can be measured.

3-5 SAMPLE TIME VARIATION

The RC time constant of an integrator is designed to provide a precise DC output for a fixed input voltage and integrating time. The formula for an operational amplifier integrator is;

$$C\,(-V_{output}) = (I_{input})\ T$$

$$T = C\,\frac{(-V_{output})}{I_{input}}$$

T is the desired integrating time.

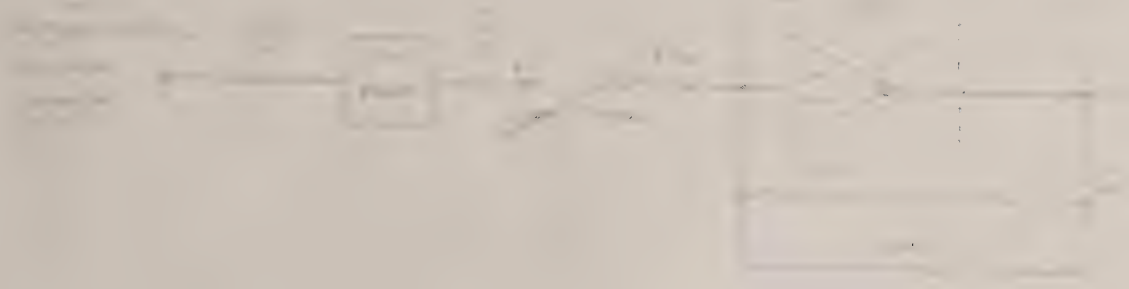
$$I_{input} = \frac{E_{input}}{R}$$

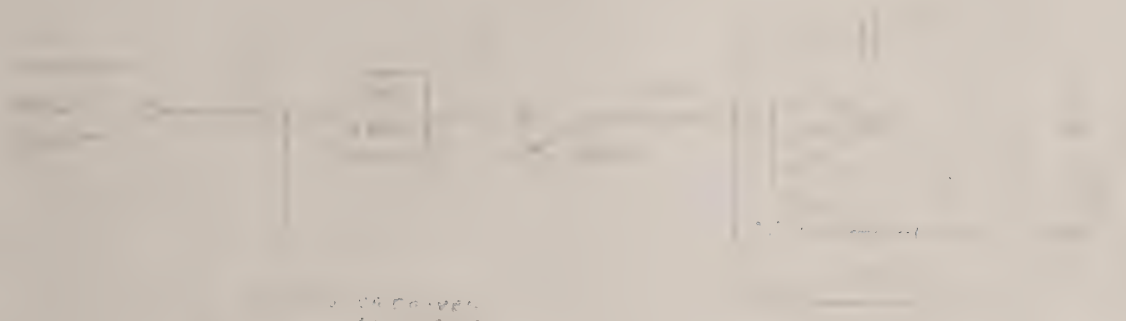
$$\therefore\ T = RC\frac{(-V_{output})}{E_{input}}$$

The most practical methods of varying integrating time are to vary C and E input. Figure X shows the methods used in the Model 202. Note; that the input signals are AC and that the synchronous detectors discussed in section 3-2 are used prior to the sample gate switches.

Relay operated decade capacitor steps provide sample time multipliers of X1, X10, and X100. The in between steps are accomplished directly by the sample time switch by using identical voltage dividers for sample time multipliers of X1, X2, and X5.

The initial R and C values are designed for 1 millisecond sample time. The possible sample times are therefore 1 through 500 milliseconds in a 1, 2, 5, 10 order. Though not shown in the figure, the 0.5 millisecond sample time is obtained by halving the capacitor values with the switch remaining in X1 position.





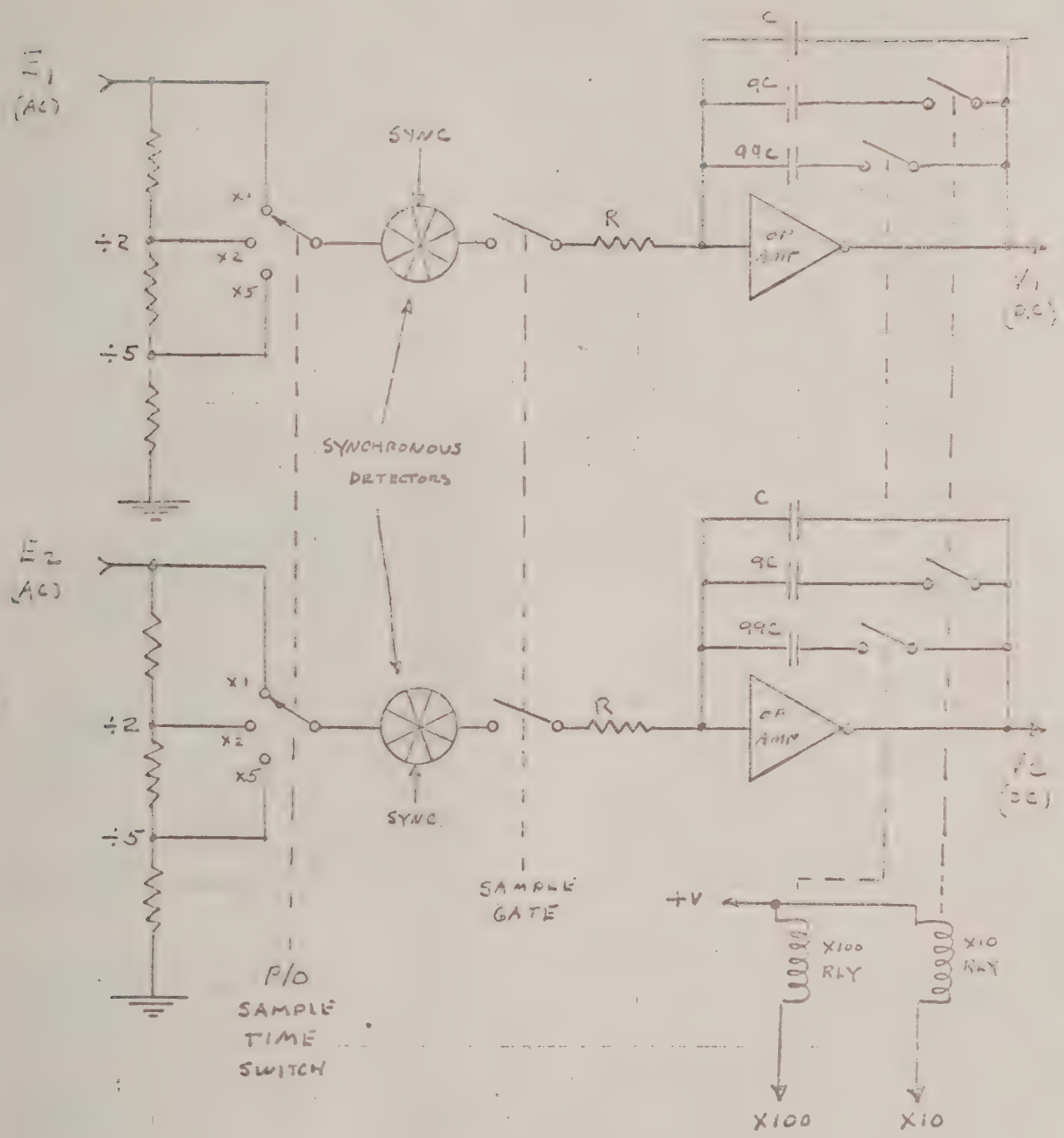


FIGURE X1

SAMPLE TIME VARIATION

3-6 BASIC VECTOR COMPONENT COMPUTER

A simplified block diagram of the Vector Component Computer is shown in figure XII with a timing diagram. Some circuits have not been included in this diagram but are discussed elsewhere. Circuits involved with sample time variation are discussed in section 3-5, inhabit and disable functions in section 3-7, differences between the Model 202 and 202A in section 3-8, and detailed operation of the computing element assemblies in sections 3-2, 3-3, and 3-4.

Operation is initiated by a trigger pulse (F) received through T1 from on external source or from the UJT Oscillator 15 in the CW mode of operation. Multivibrator 16 provides the sample delay (G) which is adjustable from the front panel to allow sampling at any point within a time bust waveform. Differentiator 17 generates the main trigger from the trailing edge of the sample delay waveform. An auxiliary trigger (X) is also available for adapters, plug-ins, or other auxiliary equipment used in conjunction with the Vector Component Computer.

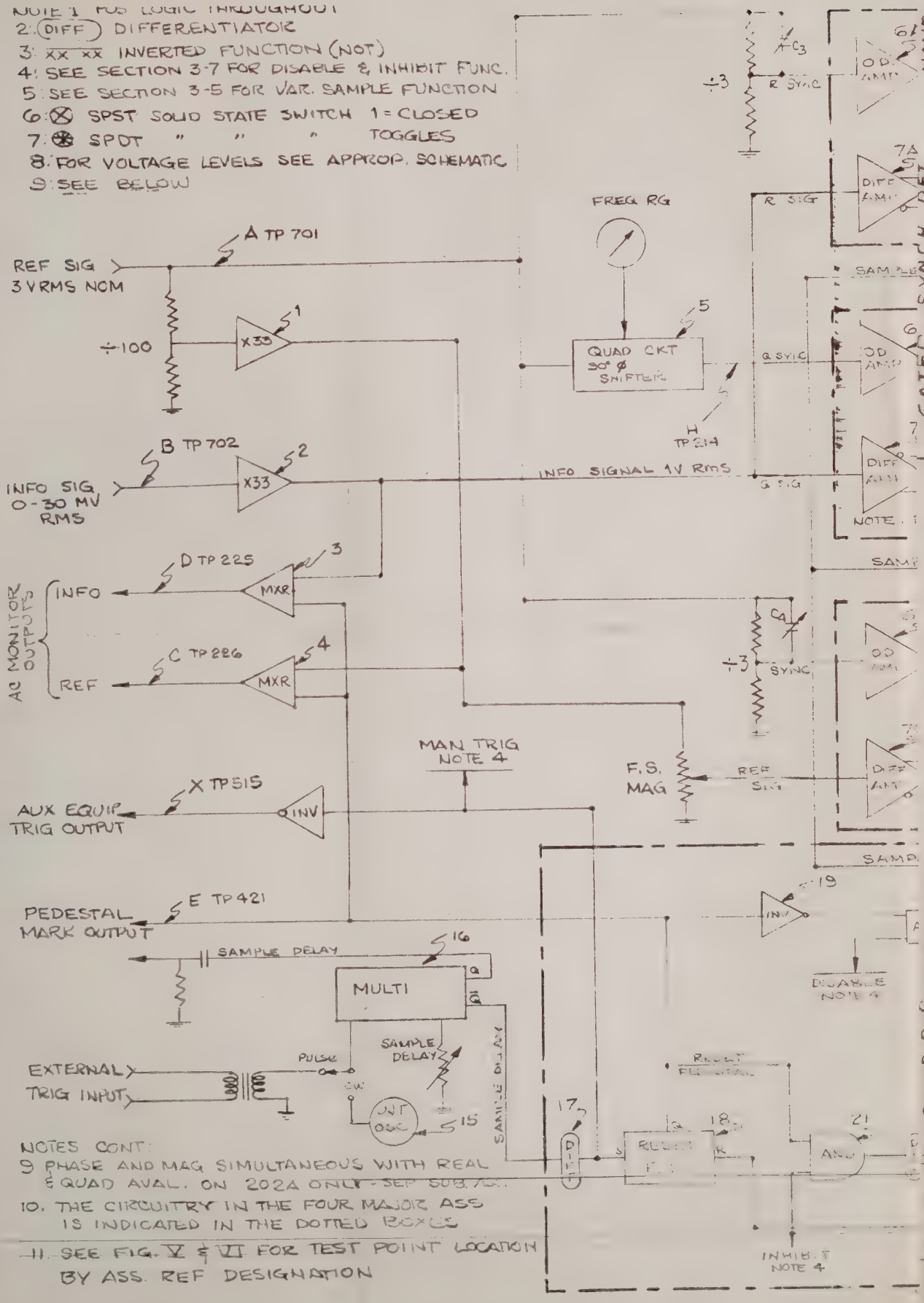
The main trigger sets the Reset flip-flop 18 whose output is the "Mark" signal for external use, the pedestal for mixing with the AC input signals for oscilloscope monitoring, and the Reset signal (E) which opens switches 12A, 12B, and 12C in readiness for the next measurement cycle and sets the start flip-flop 23. The start flip-flop allows one and only one measurement cycle per trigger pulse. It's output (M) allows the sample flip-flop 27 to be set, through AND gate 26 on the next positive going zero crossing of the reference signal. The start flip-flop 23 is reset by the leading edge of the sample gate (Q).

The Sample Gate (Q) closes solid state switches 9A, 9B, and 9C allowing the detectors to integrate their input signals. The sample gate (Q) also disables AND gate 31 through inverter 29. When the reference channel output (R) exceeds the comparator 36 set point, the compute signal (U) changes state, enabling AND gate 30. The sample flip-flop 27 is reset at the next positve going zero crossing of the reference signal, stopping the detection. When the sample gate (Q) returns to zero, AND gate 31 is enabled, generating the compute gate (V).

The compute gate (V) discharges all three integrator through R2A, R2B, R2C, until the reference output (R) returns to the comparator 35 set point. Compute signal (U) and compute gate (V) return to zero which opens switches 10A, 10B and 10C and stops the discharge.

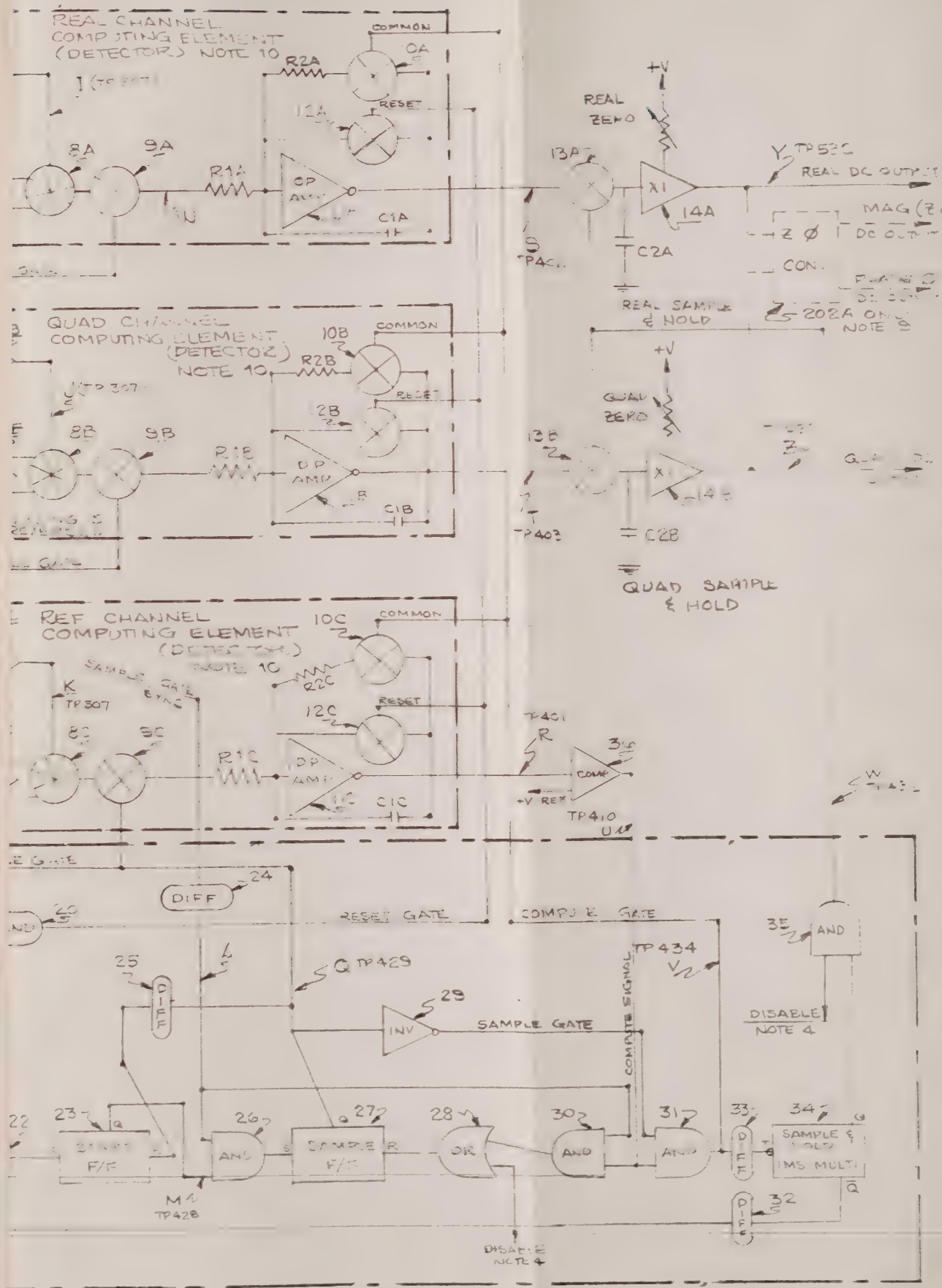
The falling edge of the Compute gate (V) through differentiator 33 triggers the sample and hold Multivibrator 34. The sample and Hold gate (W) closes solid state switches 13A and 13B allowing storage capacitors C2A and C2B to charge to the Real and Quadrature Detector output levels (S) and (T). The trailing edge of the 1 millisecond Sample and Hold Gate (W) resets the Reset flip-flop 18.

NOTE 1 POS LOGIC THROUGHOUT
2. (DIFF) DIFFERENTIATOR
3. XX XX INVERTED FUNCTION (NOT)
4. SEE SECTION 3-7 FOR DISABLE & INHIBIT FUNC.
5. SEE SECTION 3-5 FOR VAR. SAMPLE FUNCTION
6. ⊗ SPST SOLID STATE SWITCH 1 = CLOSED
7. ⊛ SPDT " " " TOGGLES
8. FOR VOLTAGE LEVELS SEE APPROP. SCHEMATIC
9. SEE BELOW

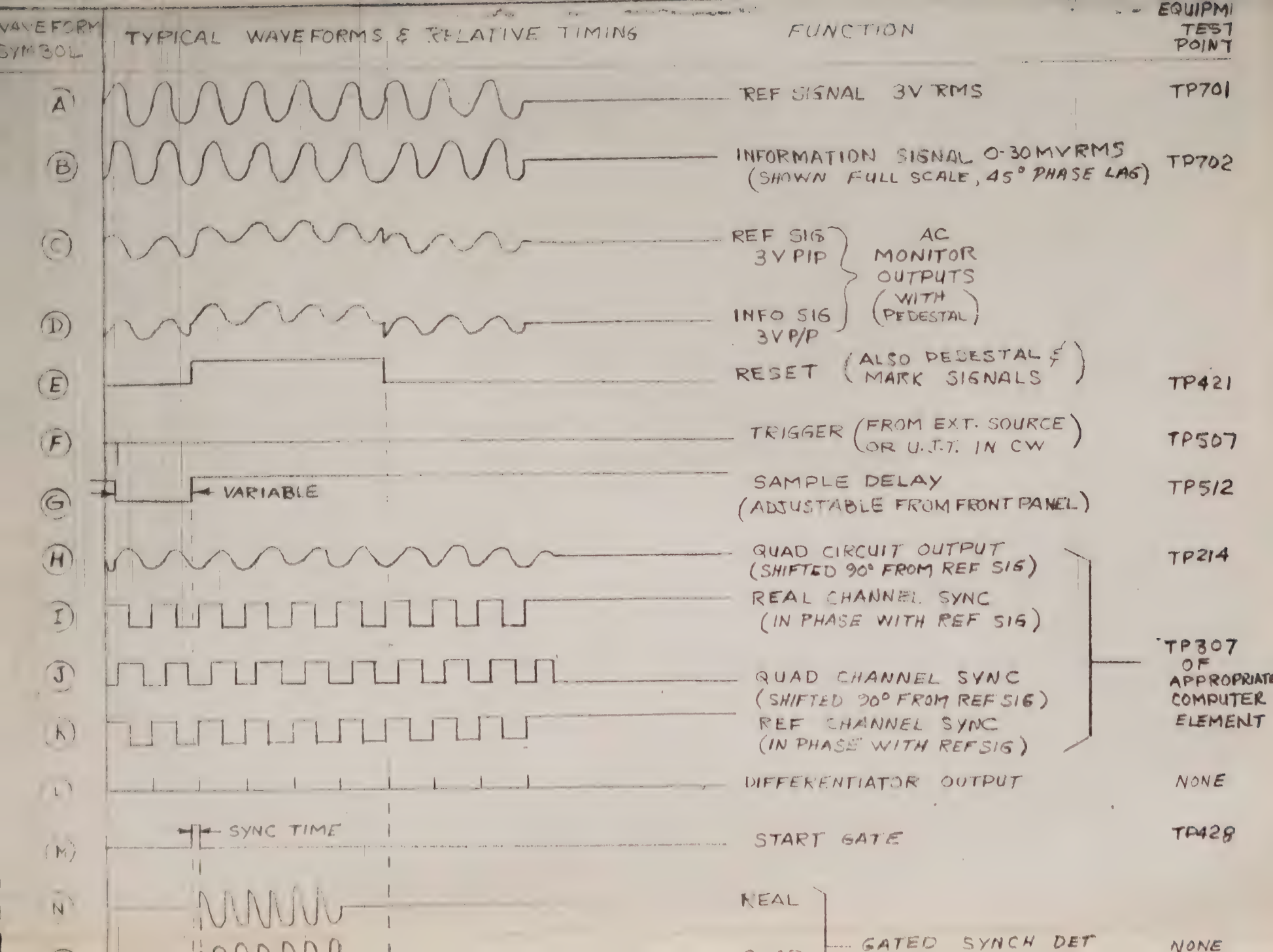


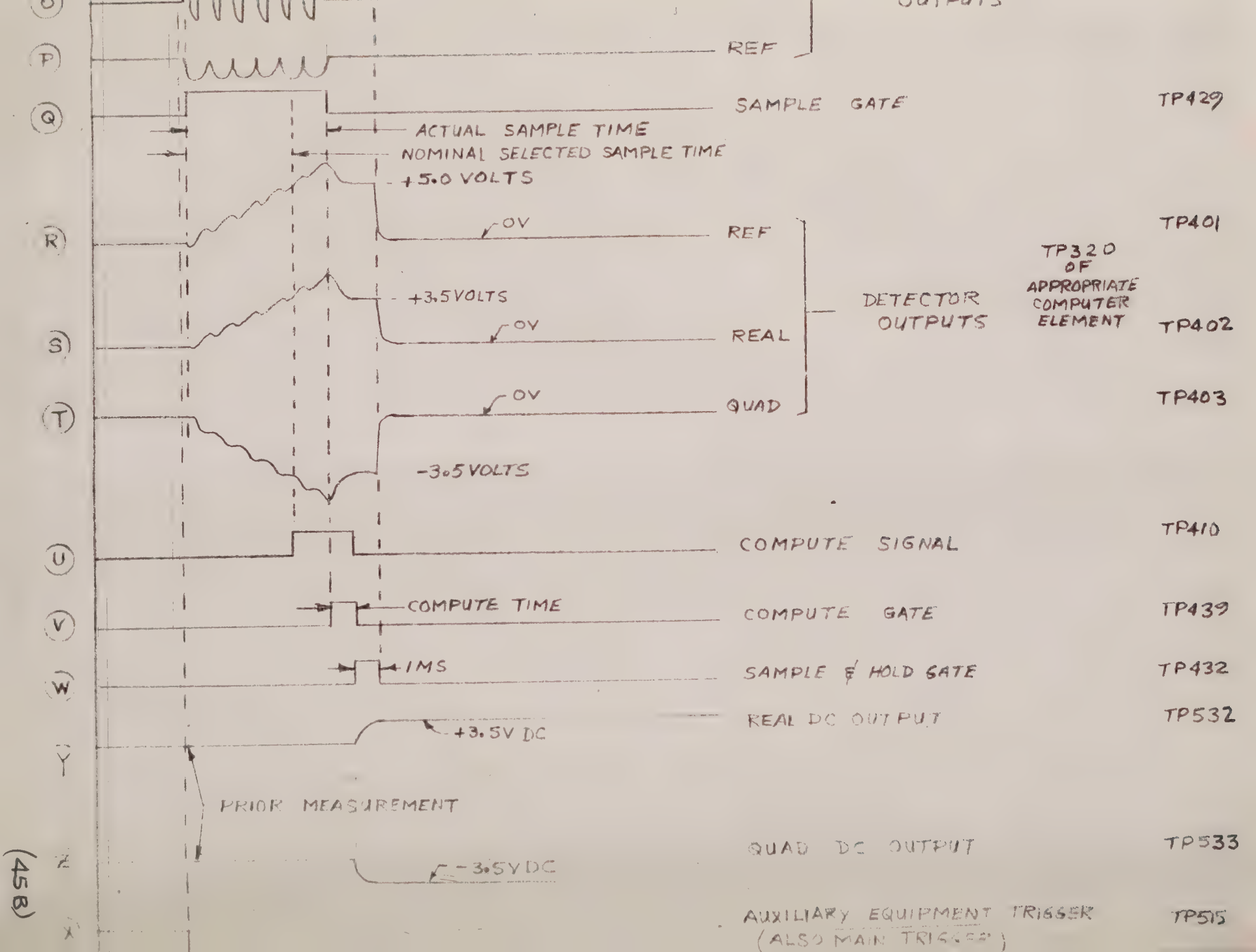
NOTES CONT:
9. PHASE AND MAG SIMULTANEOUS WITH REAL & QUAD AVAL. ON 202A ONLY - SEP 508.75.
10. THE CIRCUITRY IN THE FOUR MAJOR ASS IS INDICATED IN THE DOTTED BOXES
11. SEE FIG. V & VI FOR TEST POINT LOCATION BY ASS. REF DESIGNATION

from Greg for clarity
12.12.75 J. Stenhouse



202(A) FIGURE XI SIMPLIFIED BLOCK & TIMING DIAGRAM 100760
SHEET 1 OF 2 PAGE 45A


WAVEFORM SYMBOL
TYPICAL WAVEFORMS & RELATIVE TIMING
FUNCTION
EQUIPMENT TEST POINT
A
REF SIGNAL 3V RMS
TP701
B
INFORMATION SIGNAL 0-30MVRMS (SHOWN FULL SCALE, 45° PHASE LAG)
TP702
C
REF SIG 3V PIP
AC MONITOR OUTPUTS (WITH PEDESTAL)
D
INFO SIG 3V P/P
E
RESET (ALSO PEDESTAL & MARK SIGNALS)
TP421
F
TRIGGER (FROM EXT. SOURCE OR U.J.T. IN CW)
TP507
G
VARIABLE
SAMPLE DELAY (ADJUSTABLE FROM FRONT PANEL)
TP512
H
QUAD CIRCUIT OUTPUT (SHIFTED 90° FROM REF SIG)
TP214
I
REAL CHANNEL SYNC (IN PHASE WITH REF SIG)
J
QUAD CHANNEL SYNC (SHIFTED 90° FROM REF SIG)
TP307 OF APPROPRIATE COMPUTER ELEMENT
K
REF CHANNEL SYNC (IN PHASE WITH REF SIG)
L
DIFFERENTIATOR OUTPUT
NONE
SYNC TIME
M
START GATE
TP428
N
REAL
GATED SYNCH DET
NONE


P
REF
Q
SAMPLE GATE
TP429
ACTUAL SAMPLE TIME
NOMINAL SELECTED SAMPLE TIME
+5.0 VOLTS
R
OV
REF
TP401
TP320 OF APPROPRIATE COMPUTER ELEMENT
+3.5VOLTS
DETECTOR OUTPUTS
S
OV
REAL
TP402
T
OV
QUAD
TP403
-3.5VOLTS
U
COMPUTE SIGNAL
TP410
V
COMPUTE TIME
COMPUTE GATE
TP439
W
1MS
SAMPLE & HOLD GATE
TP432
REAL DC OUTPUT
TP532
Y
+3.5V DC
PRIOR MEASUREMENT
QUAD DC OUTPUT
TP533
Z
-3.5V DC
AUXILIARY EQUIPMENT TRIGGER
(ALSO MAIN TRIGGER)
TP515
X

3-6 BASIC VECTOR COMPONENT COMPUTER (cont)

The return of the Reset Gate (E) to zero signals the end of the detection cycle, and indicates that the Real and Quadrature DC outputs (Y) and (Z) have changed to this new value. The end of the Reset gate (E) also closes switches (12A), (12B), and (12C) through Inverter (19) and AND gate (20). The integrators are reset to zero in readiness for the next measurement cycle.

Differential Output Amplifiers (7A), (7B), and (7C) and Solid State Switches (8A), (8B), and (8C) form the synchronous detectors as discussed in section 3-2. These switches are SPDT with the output alternately connected to either the in-phase or out of phase outputs of the Differential Output amplifiers, under control of the sync signals from Overdriven Amplifiers (6A), (6B), or (6C).

The REAL channel sync is in-phase with the reference signal therefore this detector performs the function;

$$\text{Real DC Output} = \frac{\text{V info}}{\text{V ref}} \cos\phi$$

The Quadrature channel sync is shifted 90° from the reference signal by Quad Circuit (5), therefore, this detector performs the function:

$$\text{Quadrature DC OUTPUT} = \frac{\text{V info}}{\text{V ref}} \sin\phi$$

The reference channel sync is the reference signal forming simply a full wave rectifier however, with identical detection characteristics to the real and quadrature detectors. The FS MAG pot R4 allows simultaneous gain adjustment for both the real and quadrature outputs. Full scale information signal input varies around the 30 millivolt nominal with different plug-ins.

Capacitor C3, the Real channel Phase Trim, allows adjustment of the high frequency detection capability of the Real Channel by shifting the phase of the sync input. A similar trimmer C4 in the reference channel sync is used for high frequency response adjustment.

3-7 SPECIAL FUNCTIONS

Four groups of circuits not fully shown in the simplified block diagram of figure II are used in the Vector Component Computer.

One group involving the front panel FUNCTION switch sets up various arrangements of input and sync signals to the detectors to make different measurements and to allow calibration. Model 202 and Model 202A differ in these circuits

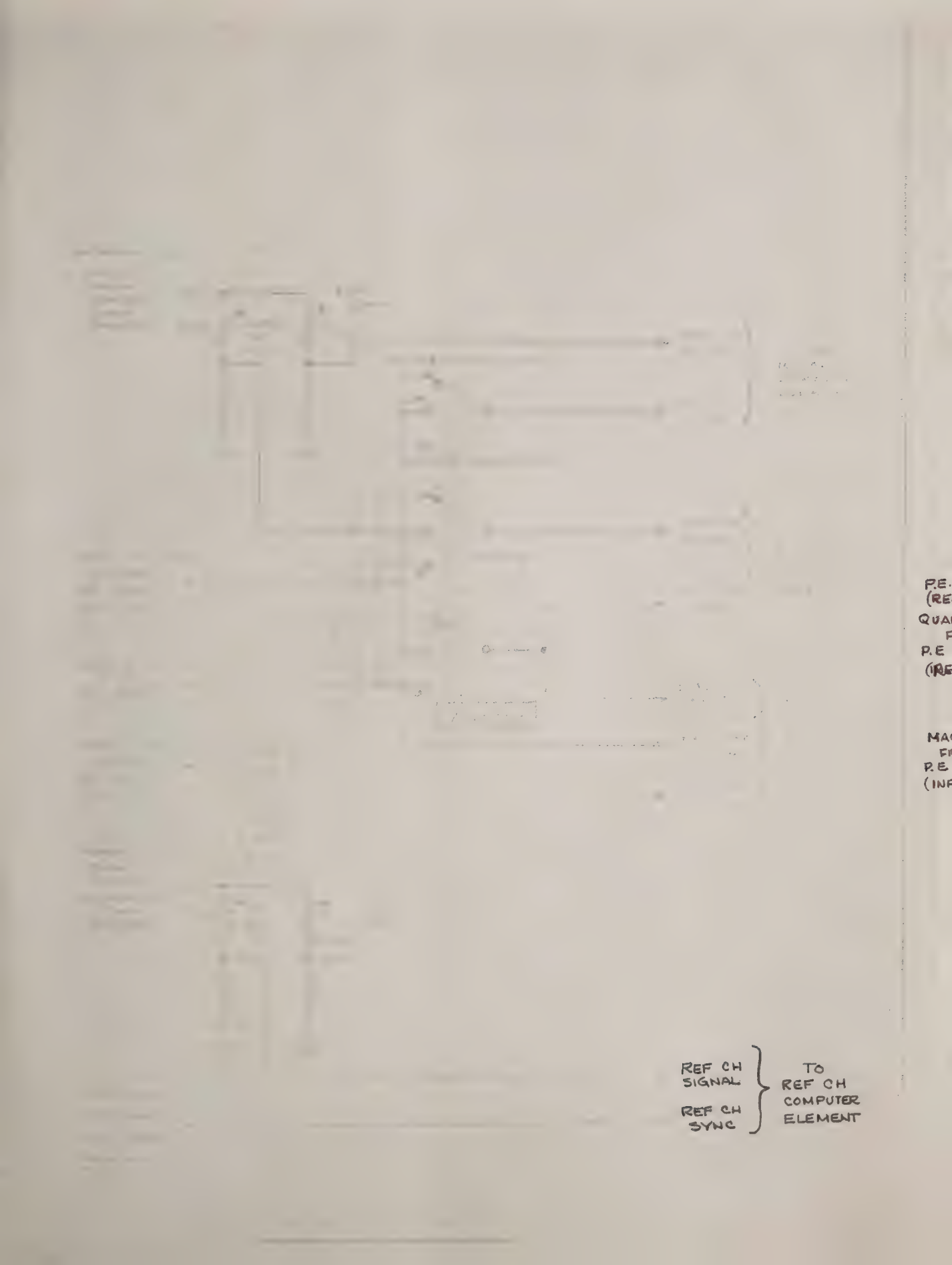
3-7 SPECIAL FUNCTIONS (cont)

The second group contained in the AC Limits Assembly measures the peak levels of various AC signals within the equipment and either inhibits operation or disables operations already in progress. A third group disables operations in progress when any one of the three detector outputs exceeds present limits.

A fourth group buffers and level shifts internally generated signals for the lighting of lights and the external synchronizing and control outputs. These are relatively simple circuits and will not be described further since the schematics are self explanatory.

A simplified schematic of the FUNCTION switch is shown in figure XII. Note; that the Model 202 and the Model 202A are different. For the Model 202 in the Vector Components position, the real channel sync is the reference signal, the quad channel signal is the information signal, and the quad channel sync is the reference signal shifted 90° in phase by the Quad Circuit. The Quad circuit is a differentiator whose output level varies with signal frequency. If the signal frequency is too low for the FREQUENCY RANGE selected on the front panel, the Quad Circuit output may be too low to properly operate the synchronous detectors. A level detector in the AC Limits assembly inhibits sampling when the Quad Channel sync is below the set point. In this FUNCTION switch position the Quad channel sync is the output of the Quad Circuit. In the Vector Magnitude position both real and quadrature channel sync signals are the information signal. Since the information signal may go to zero a possibility of loss of sync occurs. The AC Limits assembly will inhibit sampling when the information signal is less than 10% of full scale. The quad channel signal is the reference signal in this operating mode, therefore, the Quad DC output will be proportional to $-\cos \varphi$ (power factor). There is no phase adjusting network in the quad channel sync circuit therefore the output will be in error above 10 kHz and for power factors less than 0.6 The real channel is operating as a full wave rectifier in this mode so it's output is the vector magnitude. In the CAL position of the FUNCTION switch both real and quadrature channel sync are the reference signal, therefore, with a full scale information signal (in phase) the real channel output will be positive full scale (+5.00V) and the quad channel output will be negative full scale (-5.00V). (The phasing of the signals to the synchronous detector in the quad channel is reversed such that the output follows normal conventions for impedance and admittance.)

For the Model 202A the FUNCTION switch position for MEASURE is the same as the VECTOR COMPONENTS position in the Model 202. An additional assembly provides vector magnitude and phase angle simultaneously with the real and quadrative components. The magnitude and phase outputs are derived from the real and quadrature DC outputs, therefore, to calibrate these outputs the quad DC output is shorted in the CAL REAL position and the real DC output is shorted in the CAL QUAD position.


REF CH SIGNAL
REF CH SYNC
TO REF CH COMPUTER ELEMENT

REAL CH
GAIN

R122 QUAD CH GAIN R124

ASSY
SIG)
INPUT
ROM
ASSY
FSIG)

FREQ.
RG.

SYNC
OM
ASSY.
SIG)

TO
REF CHAN
COMPUTER
ELEMENT

FIGURE XII
SIMPLIFIED SCHEMATIC
FUNCTION SWITCH

3-7 SPECIAL FUNCTIONS (cont)

The second and third groups of special circuits are shown in block diagram form in figure XIII. These are the inhibit and disable circuits. The cycle of operation starts with the main trigger which resets all flip-flops to Q=O. The AC signal levels are detected by the peak detectors. If any input level exceeds the set point the appropriate flip-flop is set to Q=1. In normal operation flip-flops ⟨17⟩ & ⟨18⟩ are reset (Q=O) and flip-flops ⟨16⟩ and ⟨19⟩ are set (Q=1) almost immediately after being reset by the trigger.

The set point for the REF SIG LOW flip-flop is 2.1 V RMS referred to the input. When the reference signal exceeds this level the flip-flop is set. The REF SIG OVLD flip-flop ⟨17⟩ set point is 3.9 V RMS referred to the input. Thus the operating range for the reference signal is 3.0V RMS $\pm$ 30%.

The INF SIG OVLD flip-flop ⟨18⟩ set point is 45 MV RMS referred to the input, 30% over-range. In the Model 202 the QUAD SYNC LOW flip-flop ⟨19⟩ set point is an information signal level of 1.5 MV RMS referred to the input with the FUNCTION switch in "Vector Magnitude", this corresponds to approximately 5% of full scale. In the Model 202A this adjustment is made in the "Measure" mode with an input frequency 0.7 times the lowest frequency indicated on the FREQ. RANGE switch. In the "Vector Components" mode of the Model 202 and the "Measure" mode of the Model 202A the quad sync is connected to the Quad Circuit output. (see preceeding paragraphs)

Level detectors ⟨1⟩ and ⟨3⟩ are connected through isolation diodes to all three detector output signals (Ⓡ, Ⓢ, and Ⓣ of figure XI). Therefore any detector output exceeding + or -7.5 volts will provide an output through OR ⟨2⟩.

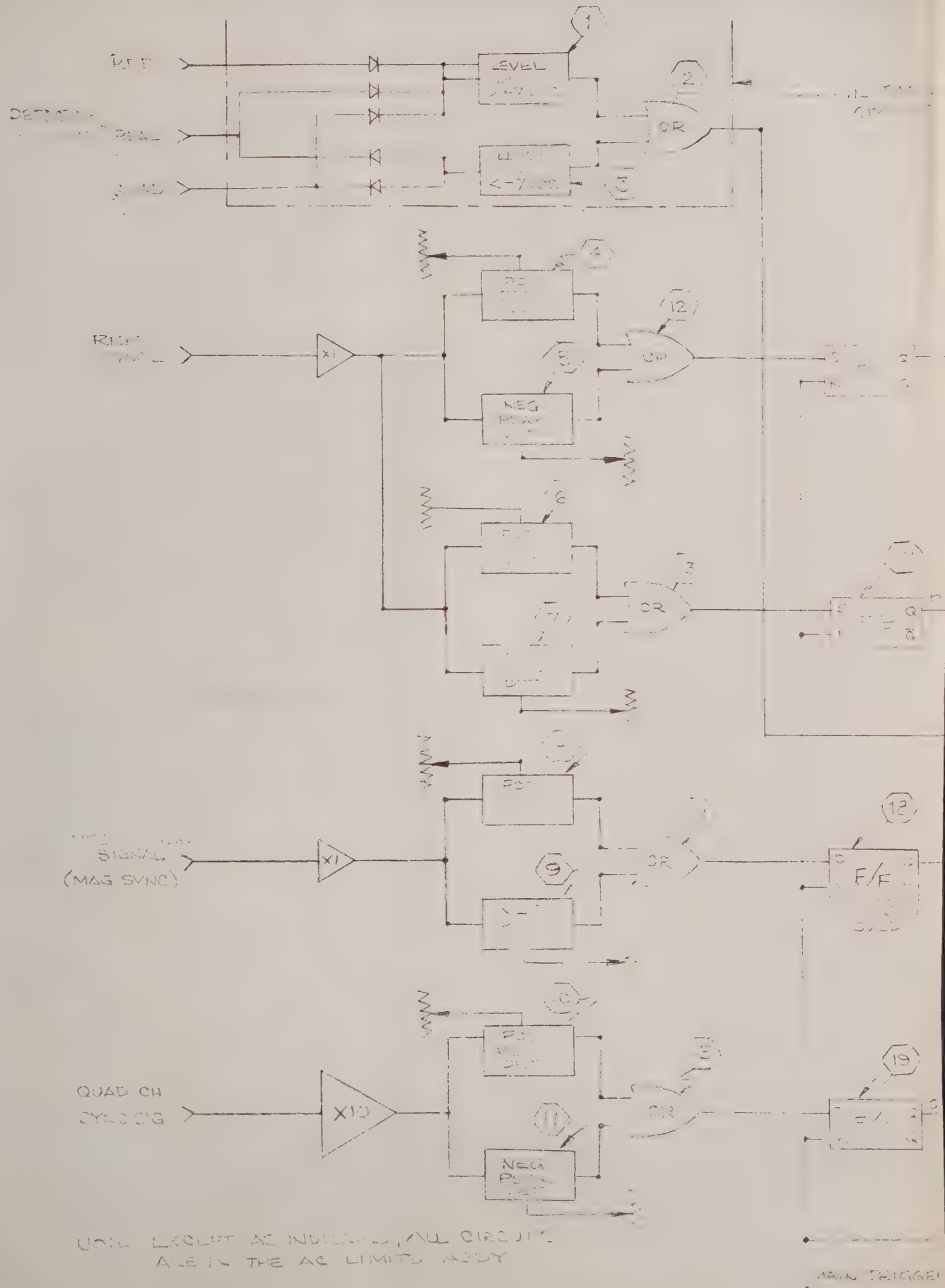
An output from OR ⟨2⟩, FF ⟨17⟩ or FF ⟨18⟩ will set disable flip-flop ⟨23⟩. The disable output performs several functions; it causes immediate reset of the detectors through AND ⟨20⟩ of figure XI, it turns off the sample gate immediately through OR ⟨28⟩ of figure XI, it prevents data change in the sample and holds through AND ⟨35⟩ of figure XI, and it lights the OUT OF LIMITS light on the front panel.

The equipment is disabled and the preceeding data held under the following conditions;

1. Reference of information signal overload after the sample delay only.

2. Detector overload due to too low a frequency for the sample time selected.

3. Detector overload due to loss of signal before completion of a measurement cycle.


LEVEL
OR
NEG
OR
NEG
F/F
OR
X10

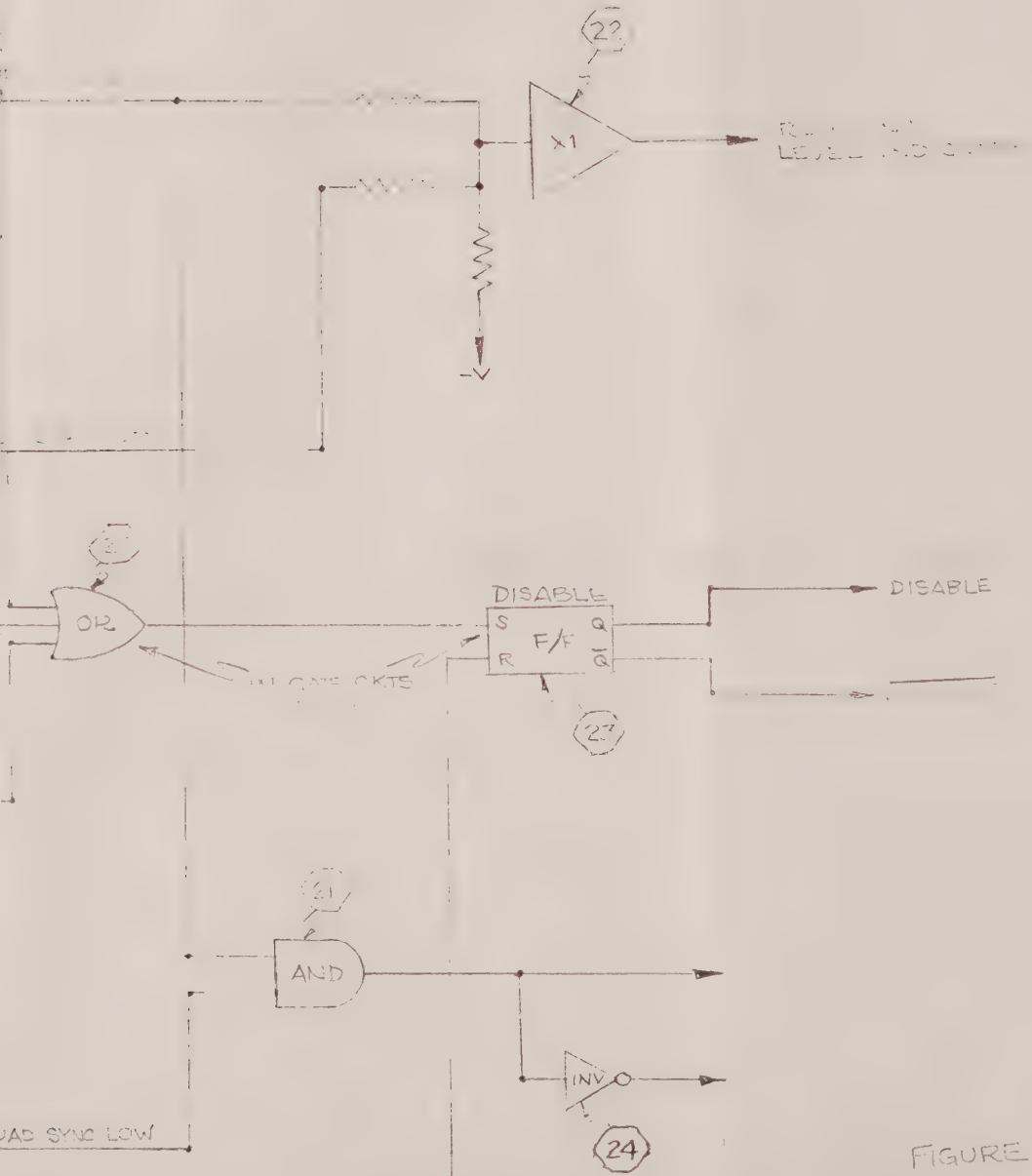


FIGURE XIII

SIMPLIFIED BLOCK DIAGRAM
INHIBIT AND DISABLE CIRCUITS

3-7 SPECIAL FUNCTIONS (cont)

When the main trigger resets flip-flop (16) and (19) the start flip-flop (23 of figure XI) is inhibited by AND (21) of figure XI until both the reference signal and the quad sync signal have exceeded their set levels to generate the INHIBIT (not inhibited) output through AND (21) of figure XI.

Buffer amplifier (22) provides a GO-NO GO signal useful in some system applications. The output is zero when the reference signal is within limits, minus if low and plus if overloaded. A meter, lights or a simple servo might be connected to this output.

3-8 MODEL 202A MAGNITUDE & PHASE CIRCUIT

The function of the coordinate converter assembly in the Model 202A is to convert the real and quadrature DC outputs (rectangular coordinates) to phase angle and magnitude DC outputs (polar coordinate). The basic principle used is to convert the DC inputs to AC sinusoidal signals and then measure the amplitude and phase of the resultant.

Figure XIV is a simplified block diagram of the coordinate converter. A 21. kHz oscillator provides differential outputs to toggle two ÷ 2 flip-flops. The flip-flops are toggled on opposite edges of the oscillator output therefore their outputs are square waves at 10.5 kHz but with 90° phase difference. The flip-flop outputs operate switches which chop the real and quadrature DC output signals. Filtering the resulting square waves results in sine wave signals whose amplitudes are proportional to the appropriate DC inputs but with the quadrature signal shifted 90° in phase. These AC signals are vectorily added in the mixer composed of R1A, R1B, R2 and the operational amplifier.

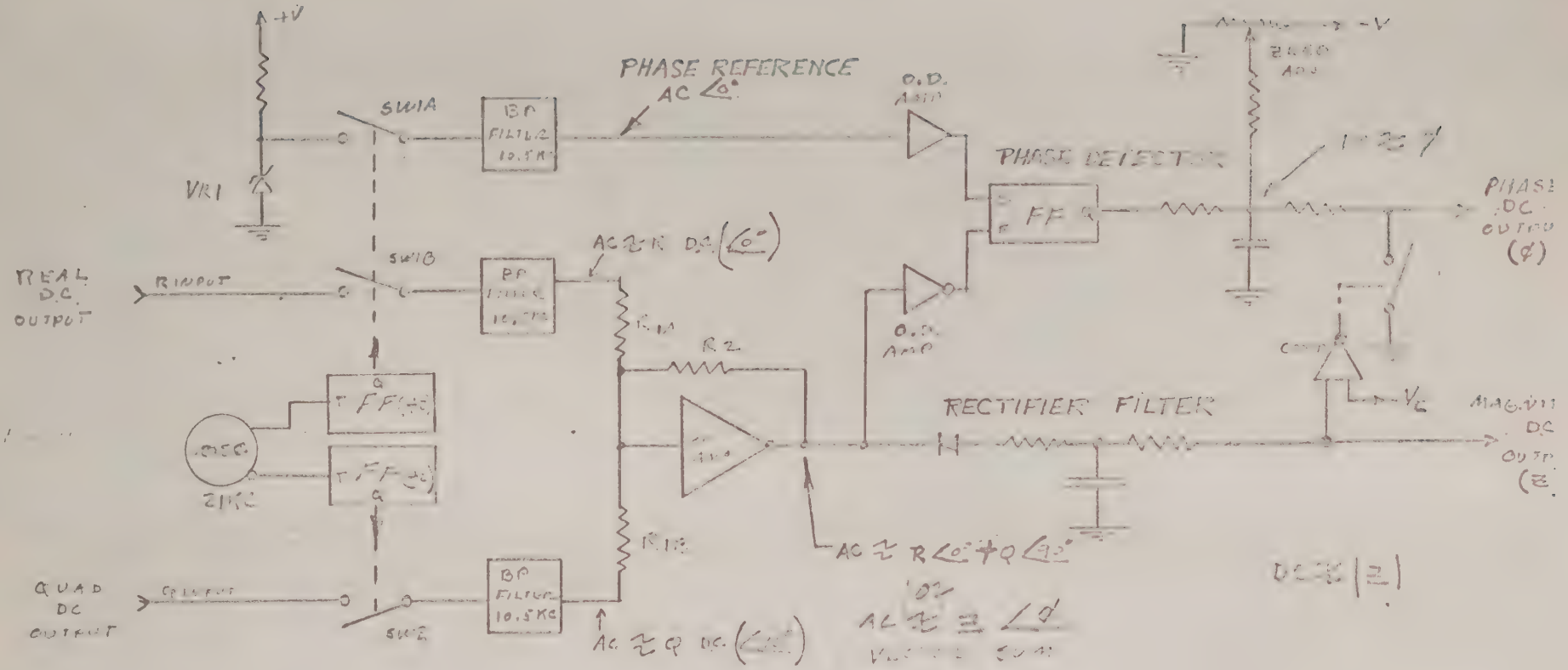
A phase reference signal is also generated by SW1A which chops a fixed DC from zener diode VR1. The filtered AC is in phase with the AC signal developed in the R channel and is therefore the 0° phase reference.

The output of the mixer is the vector addition of the R signal at an angle of 0° and the Q signal at an angle of 90°. A simple rectifier-filter provides a DC output proportional to the vector magnitude (Z) of the real and quadrature DC signals.

The phase detector is a flip-flop which is set (Q=1) by the positive going transition of the phase reference signal and reset (Q=0) by the negative going edge of the vector sum signal generated previously. The output of the flip-flop is a 50% duty cycle square wave when the phase is 0°. This occurs for a positive real input and a zero quadrature input. The average value of the flip-flop output is 50% of full scale and varies from zero to full scale. A negative bias is supplied via the Zero Adj. pot which sets the output to zero volts DC for zero degrees and can be calibrated for angles approaching ± 180°.

3-8 MODEL 202A MAGNITUDE & PHASE CIRCUIT (cont)

When both inputs are zero no vector sum is generated and the phase detector locks up at a false indication. A comparator senses the magnitude output and shorts the phase output to ground.



(53)

FIGURE XIV

SIMPLIFIED [illegible] DIAGRAM

CONVERTER

SECTION IV

MAINTENANCE

4-1 CHECKOUT PROCEDURE

Checkout can be accomplished with any Dranetz plug-in unit or adapter. Each plug-in or adapter has two calibrate positions, full scale and zero. The full scale position provides an AC signal to it's information signal output terminal equal to the full scale output under measurement conditions. This signal is in phase with the reference signal. In the zero position a zero signal is provided however an output may result due to improper grounding of equipment. This can be verified by observing the information signal at the AC OUTPUT connector (on the rear panel) with an oscilloscope. The nominal full scale is 3V peak to peak, therefore, a signal of 30 millivolts peak to peak is 1% zero error. Since most zero error signals are due to capacitive coupling or magnetic pick-up, this error shows mostly in the quadrature output and is large at high frequencies. A high resistance ground connection from too light a grounding conductor would show in the real output and normally is a function of load current and is not dependent upon frequency with a resistive load.

Checkout should normally be done with CW signals, to preclude problems with external triggering and synchronization needed for tone burst operation. A two step process is recommended, first without the load or the device under test connected and the second simulating the conditions of measurements. By observing the information signal output on an oscilloscope in the ZERO CAL position, with and without a load the errors indicator above may be corrected or a measure of their magnitude determined such that measurement data may be corrected.

The recommended procedure is as follows:

1. Place the equipment in the CW mode.

2. Set the sample time to 10 milliseconds.

3. Set the frequency range to 3-30 kHz.

4. Set the sample delay to approximately 1 millisecond.

5. Set the signal frequency to 10 kHz.

6. Set the Function switch to either "Vector Components" or "Measure."

7. Set the mode switch on the plug-in or adapter to "Zero Cal."

8. Set the signal drive level for a 3V RMS reference signal. This can be done by measureing with an AC Voltmeter at the "3VAC Meter Output" at the Auxiliary output connector at the rear panel or by observing the "Reference Signal Output" at the "AC outputs" connector for approximately 3V peak to peak.

4-1 CHECKOUT PROCEDURE (cont)

9. The "GO" light should be on and the indicators connected to the DC outputs should all read approximately zero. The pedestal on the reference signal AC output should be approximately 12 MS wide.

10. Decrease the reference level until the "GO" light goes out. This should occur at less than 2.4 V RMS or peak to peak if using the oscilloscope.

11. Increase the reference level until the "OUT OF LIMITS" light comes on. This should occur at greater than 3.4 V RMS.

12. Decrease the reference level until the "OUT OF LIMITS" light just goes out. Turn the mode switch on the plug-in to "FS CAL". The "OUT OF LIMITS" light should remain off.

13. The real and magnitude (202A) outputs should be approximately full scale and the quadrature and phase (202A) outputs near zero.

14. Vary the reference level between the lower and upper limits while observing the DC outputs. The output variations should be less than 1/2% of full scale. Return the reference to 3V.

15. Change the signal frequency to 1 kHz. The "GO" light should go out.

16. Calibrate the equipment as indicated in section 2-3 for the appropriate equipment (202 or 202A) using as signal frequency near the upper end of your typical test band and the desired sample time.

17. With the Function switch in "Vector Components" or "Measure" observe the output indications in "FS CAL" and "Zero CAL" with and without the load connected to the plug-in. The variation between readings should be less than 1% of full scale or $\pm 1°$.

4-2 ADJUSTMENT PROCEDURES

The various adjustments required for alignment or maintenance all shown in figures XV and XVI and the procedures for adjustment are indicated below. Some adjustments are made at frequencies beyond the capabilities of many plug-ins used as signal sources. No adjustment in the field is then possible.

4-2A FRONT END ASSEMBLY, FIGURE XV

C706 Real Channel Phase Trim

A trimmer capacitor which shifts the phase of the real channel sync signal. This adjustment is made in the 100 to 300 kHz frequency range and is ineffective below 30 kHz. It is normally a factory adjustment made by applying a quadrature information signal and adjusting for minimum output of the real DC output.

C707 Frequency Response Trim

A trimmer capacitor which shifts the phase of the reference channel sync signal. This adjustment is made in the 100 to 300 kHz frequency ramp and is ineffective below 30 kHz.

4-2 B COORDINATE CONVERTER ASSEMBLY, FIGURE XVI

It is not recommended that adjustments be made in the field in this assembly. Factory assistance is available through the Technical Services Dept. if maintenance is required for this assembly.

4-2C TIMING AND OUTPUT ASSEMBLY, FIGURE XVI

R507 CW Repetition Rate Adjustment

A potentiometer controlling the fastest repetition rate in the CW mode of operations. It is nominally set for 30 MS between measurements with a 1 MS sample time and a 10 KC signal frequency.

R576 & R578 Real and Quad Zero Trim

Potentiometers for coarsely adjusting the zero outputs with the front panel controls centered.

4-2D COMPUTING ELEMENT ASSEMBLIES, FIGURE XVI

R305 A, B & C Zero Crossing Detector Bias Adjustments

Potentiometers for adjusting the firing point of the schmidtt trigger circuit in the ZCD module (U303). This is accomplished by monitoring at TP 307 with a tone burst signal applied. Repetition Rate = 300 MS, Pulse Width 30 KC, Sample Time = 10 MS, Sample Delay= approx 10 MS, Frequency = 10 MC, Mode = Vector Components or Measure Zero Cal signal input. It is important that the equipment be on for a sufficient time to reach normal operating temperature. Sync the oscilloscope on the external trigger. A 30 MS burst of square waves at 10 kHz should be followed by some random switching. Adjust R305 for the ZCD output to recover to the low level (+4V) before the next burst of signal.

4-2D COMPUTING ELEMENT ASSEMBLIES, FIGURE XVI (cont)

Note: Adjustments of R309 & R314 in the reference channel computing element are made by swapping the real and reference channels temporarily.

R309 A, B & C Balance Adjustment

Potentiometers for adjusting the output of the differential amplifiers in the DSD module U304. Mode=CW, Signal Frequency = 10 kHz, Sample Time = 10 MS, Assembly on extender cards. Adjust for identical low and high levels by monitoring at TP311 and TP312 with an oscilloscope. This adjustment is not necessary unless a DSD (U304) or SSS (U308) module has been changed.

R314 A, B & C Detector Zero Adjust

Potentiometers for balancing coupling capacitor leakage or SSS (U308) switch leakage. Mode=CW, Signal Frequency=1 kHz Sample Time=100 MS, Vector Components or Measure Mode, & Zero Cal. Zero Real & Quad outputs with front panel controls. Switch to 500 MS sample time. Adjust R314 for zero output of appropriate channel. Repeat at 100 MS & 500 MS, adjusting front panel controls and R314 respectively. Change frequency to 10 kHz, check that all sample times from 1 to 500 MS have the same zero output levels. The 0.5 MS time may have 1% of full scale error.

C318 A, B & C High Frequency Zero

It is not recommended that adjustments of this trimmer be made in the field. Variation of high frequency zero with component or module change is less than 1%.

4-2E AC LIMITS ASSEMBLY, FIGURE XVI

R242 & R245 Quad Sync Low (202A only)

Place the AC limits board on the extenders, function switch to measure, frequency range to 1-10 kHz, CW mode, 100 MS sample time, plug-in to F.S. cal, apply 3 V RMS at 700 Hz to reference channel input. Check at TP 209 for a waveform returning to zero. Turn R242 two turns CCW scope to TP218. Adjust R245 for a waveform returning to zero, "GO" light should be "ON". Vary frequency from 1000 Hz and trim R245 for no "GO" light at approximately 700 Hz. Turn R245 exactly one turn CW. Adjust R242 as above. Turn R245 one full turn CCW.

R242 & R245 Quad Sync Low (202only)

Place the function switch to Vector Magnitude, CW mode, 100 MS sample time, plug-in to Measure. Provide a load impedance or admittance of 7% of full scale using a capacitive load. Turn R242 two turns CCW. Vary the signal frequency for 20% of full scale. Vary the frequency to decrease the signal level and adjust R245 such that the "GO" light goes out at 7% of full scale. Turn R245 exactly one full turn CW. Adjust R242 as above. Turn R245 one full turn CCW.

4-2E AC LIMITS ASSEMBLY, FIGURE XVI (cont)

R 205 & R208 Reference Signal Low

Function switch to CAL Real or Cal, plug-in to FS Cal. Turn R205 two turn CCW. Set the reference signal level to 3.0V RMS. Adjust R 208 such that the "GO" light goes out for a reference signal level less than 2.1V RMS. Turn R 208 exactly one turn CW. Adjust R205 as above. Turn R208 one turn CCW.

R 215 & R 218 Reference Signal Overload

Adjust R 205 & R 208 as above. Turn R215 fully CCW. Adjust R218 for the OUT OF LIMITS light on for a reference signal level greater than 3.9 V RMS. Turn R218 exactly one turn CW, Adjust R215 as above, Turn R215 one turn CCW.

R257 & R260 Information Signal Overload

Function switch to Vector Components or Measures, plug-in switch to Measure. Adjust the Reference level to 2.5 V RMS. Provide a load of two times full scale. Place the AC Limits board on the extenders. Monitor at TP224. Turn R257 fully CCW. Increase the Reference level and adjust R260 for TP224 high (+12V) for reference signal levels greater than 3.0 V RMS. (Note: the OUT OF LIMITS light will be on for all of these tests.) Turn R260 exactly one turn CW. Adjust R257 as above. Turn R260 one turn CCW.

4-2F FRONT PANEL ASSEMBLY, FIGURE XVI

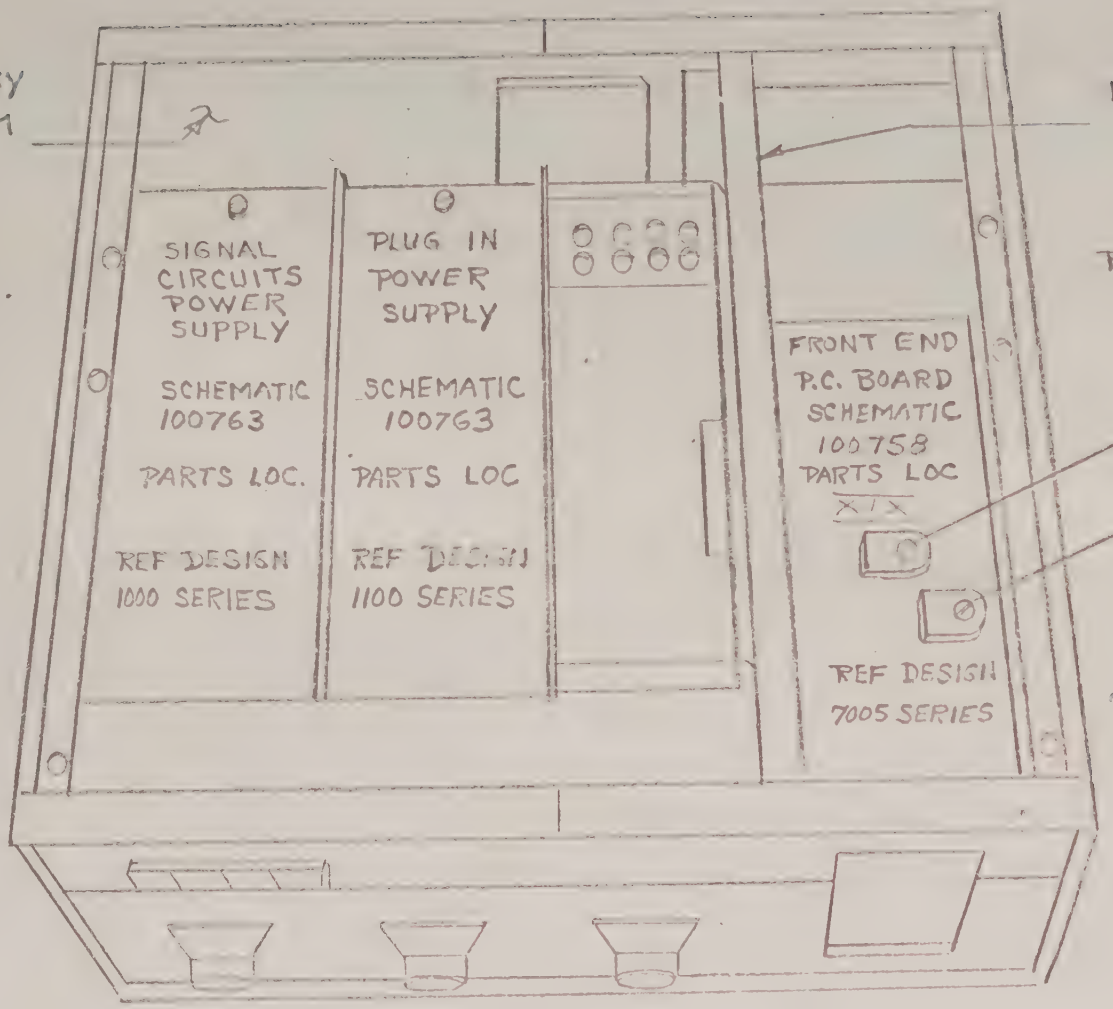
R122 & R124 Quad & Real Channel gain adjustments

Potentiometers which control the gains of the Quad & Real channels. Sample time=10 MS, Signal Frequency = 10 kHz, CW mode, zero all outputs, full scale cal. The Model 202 should be in "CAL", the Model 202A must be switched between "CAL REAL" and "CAL QUAD". Measure the Real and Quad DC outputs with the same DC Voltmeter. Adjust the "FS MAG" control for exactly 5.00 Volts output from whichever channel has the lower output level. The "FS MAG" pot should have at least 2% variation (100 MV) in each direction if not readjust the "COMP LEVEL" on the rear panel. Reduce the gain of the appropriate channel for indentical 5.00 Volt outputs.

4-2G GATE CIRCUITS ASSEMBLY, FIGURE XVI

R419 S & H Time Adjustment

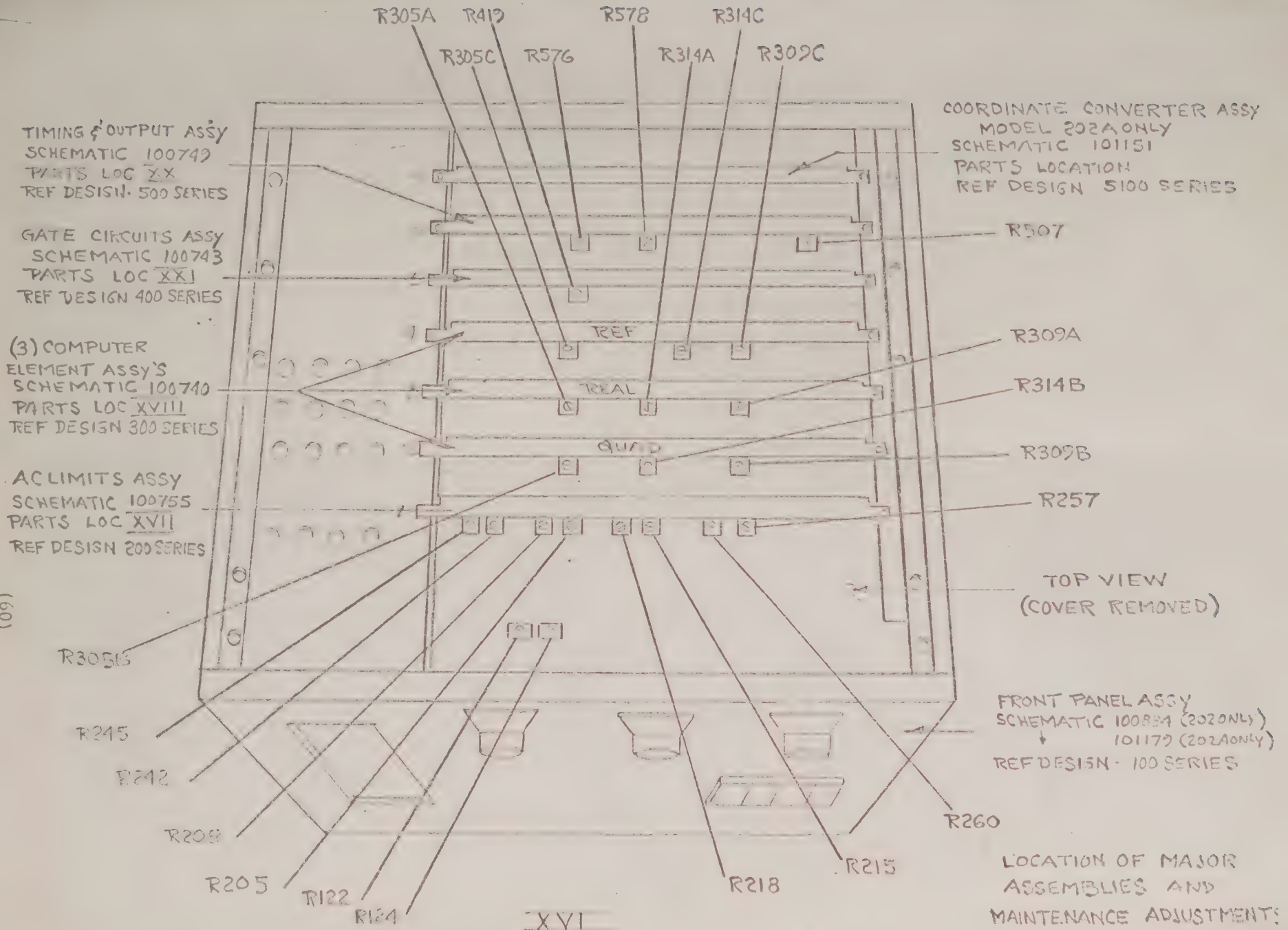
Potentiometer for adjusting the sample & hold gate to approximately 1 MS. This adjustment is made with the Gate Circuits Assembly on the extenders and an oscilloscope connected to TP423.



FRONT PANEL ASSY
SCHEMATIC 100884 - (202 ONLY)
↓ 101179 - (202A ONLY)
REF DESIGN 100 SERIES

FIG XV

LOCATION OF MAJOR ASSEMBLIES
AND MAINTENANCE ADJUSTMENTS


R305A
R419
R578
R314C
R305C
R576
R314A
R302C
TIMING & OUTPUT ASSY
SCHEMATIC 100749
PARTS LOC XX
REF DESIGN 500 SERIES
GATE CIRCUITS ASSY
SCHEMATIC 100743
PARTS LOC XXI
REF DESIGN 400 SERIES
(3) COMPUTER
ELEMENT ASSY'S
SCHEMATIC 100740
PARTS LOC XVIII
REF DESIGN 300 SERIES
AC LIMITS ASSY
SCHEMATIC 100755
PARTS LOC XVII
REF DESIGN 200 SERIES
COORDINATE CONVERTER ASSY
MODEL 202A ONLY
SCHEMATIC 101151
PARTS LOCATION
REF DESIGN 5100 SERIES
R507
R309A
R314B
R309B
R257
TOP VIEW
(COVER REMOVED)
REF
REAL
QUAD
R305B
R215
R212
R209
R205
R122
R124
R218
R215
R260
FRONT PANEL ASSY
SCHEMATIC 100834 (202 ONLY)
101179 (202A ONLY)
REF DESIGN - 100 SERIES
LOCATION OF MAJOR
ASSEMBLIES AND
MAINTENANCE ADJUSTMENTS

4-3 TROUBLE SHOOTING PROCEDURE

A familiarity with the theory of operation is required to troubleshoot the equipment. Figures X, XI, and XII can be used for most problems encountered. The most significant waveforms are the outputs of the Computing Element Assemblies at TP320 of the appropriate assembly.

Actual voltage levels on the schematics are indicated for C W operation, 10 MS sample time, 10 kHz signal frequency, full scale cal signal applied, approximately 1 MS sample delay, with the Model 202 in "CAL" or the Model 202A in either "CAL REAL" or "CAL QUAD" as is appropriate.

Use of the Checkout procedure of section 4-1 is recommended to aid in isolating faults. Once the problem is isolated to an assembly the alignment procedure for that assembly should be performed as many difficults can be cured by simple readjustment.

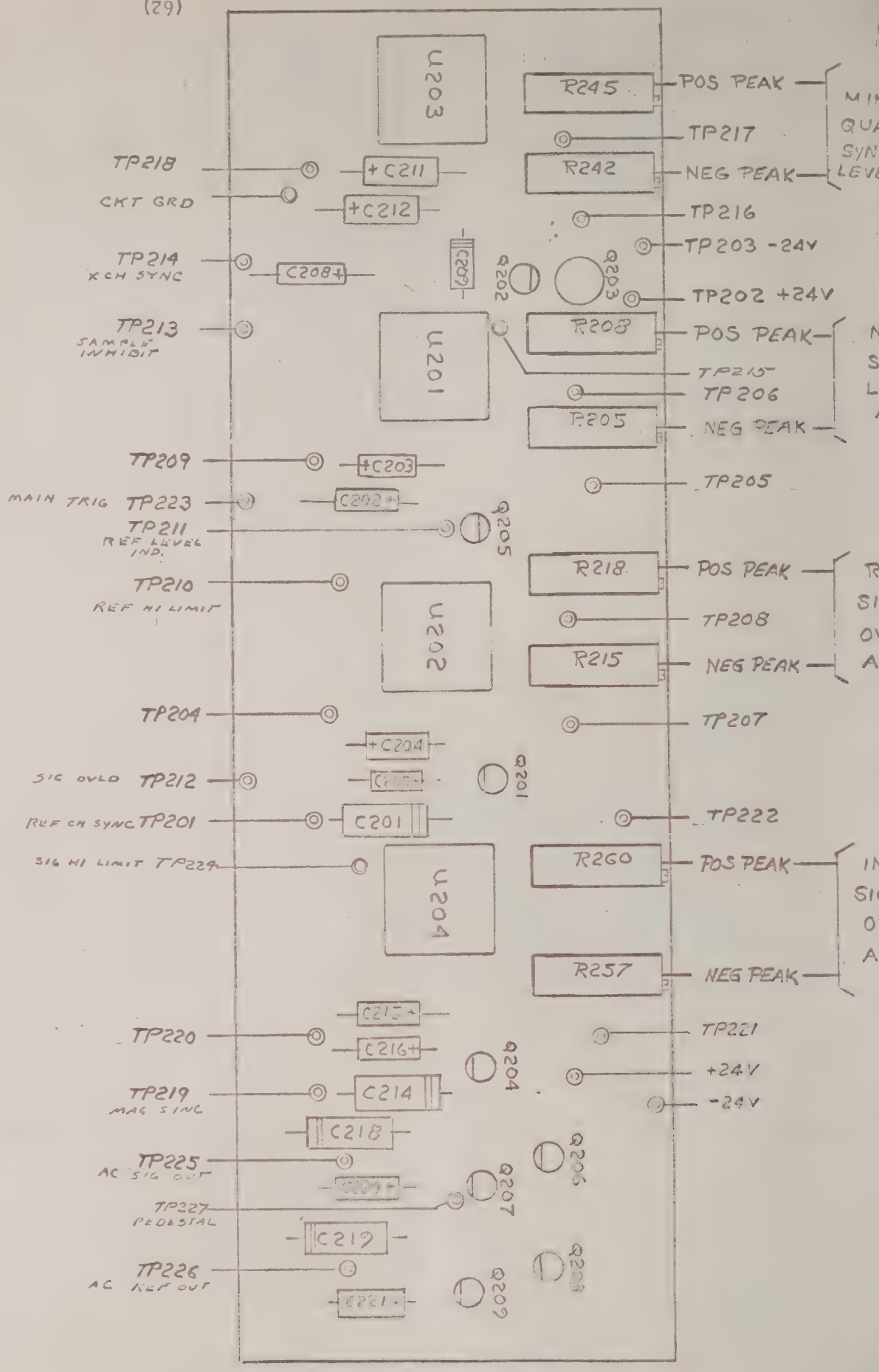
Reliability analysis indicates the most probable failures will occur within a module in the Compute Element Assembly. Swapping of assemblies can isolate problems to a particular assembly however the quad channel is phased differently than the reference and real channels.

Temporary swapping of modules is another troubleshooting aid particularily for intermittent type problems. The ZCD modules are not swappable without bias readjustment. It is suggested that modules be marked with their original location such that they may be returned after fault location to avoid need for realignment in the unaffected channels.

Problems of unstable or noisy readings particularily during time burst measurements results from high noise levels, bias shifts causing signal distortion and clipping or improper adjustment of ZCD bias.

Low power line voltage might cause high internal noise of low frequency related to some external equipment turning on and off.

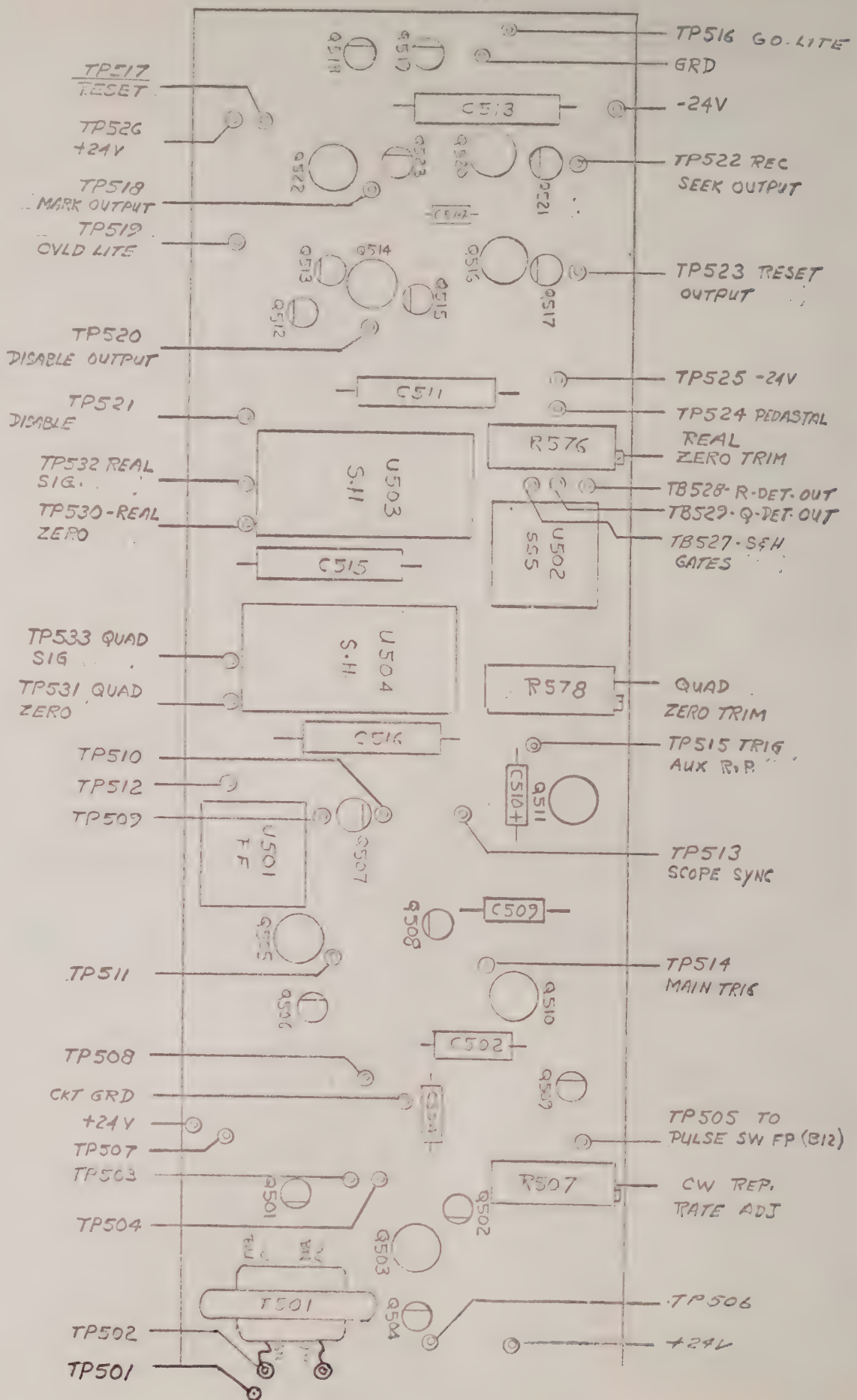
High internal temperatures might be the result of high line voltage, poor rack ventilation, or plugging of the air intake and exhaust ports (located on the top surface.) Internal temperature rise is normally 30°F above ambient. Intake air temperatures above 110° F might cause intermittent instability or noise particularily after the equipment has been on for one or two hours.



AC LIMITS CKT BOARD

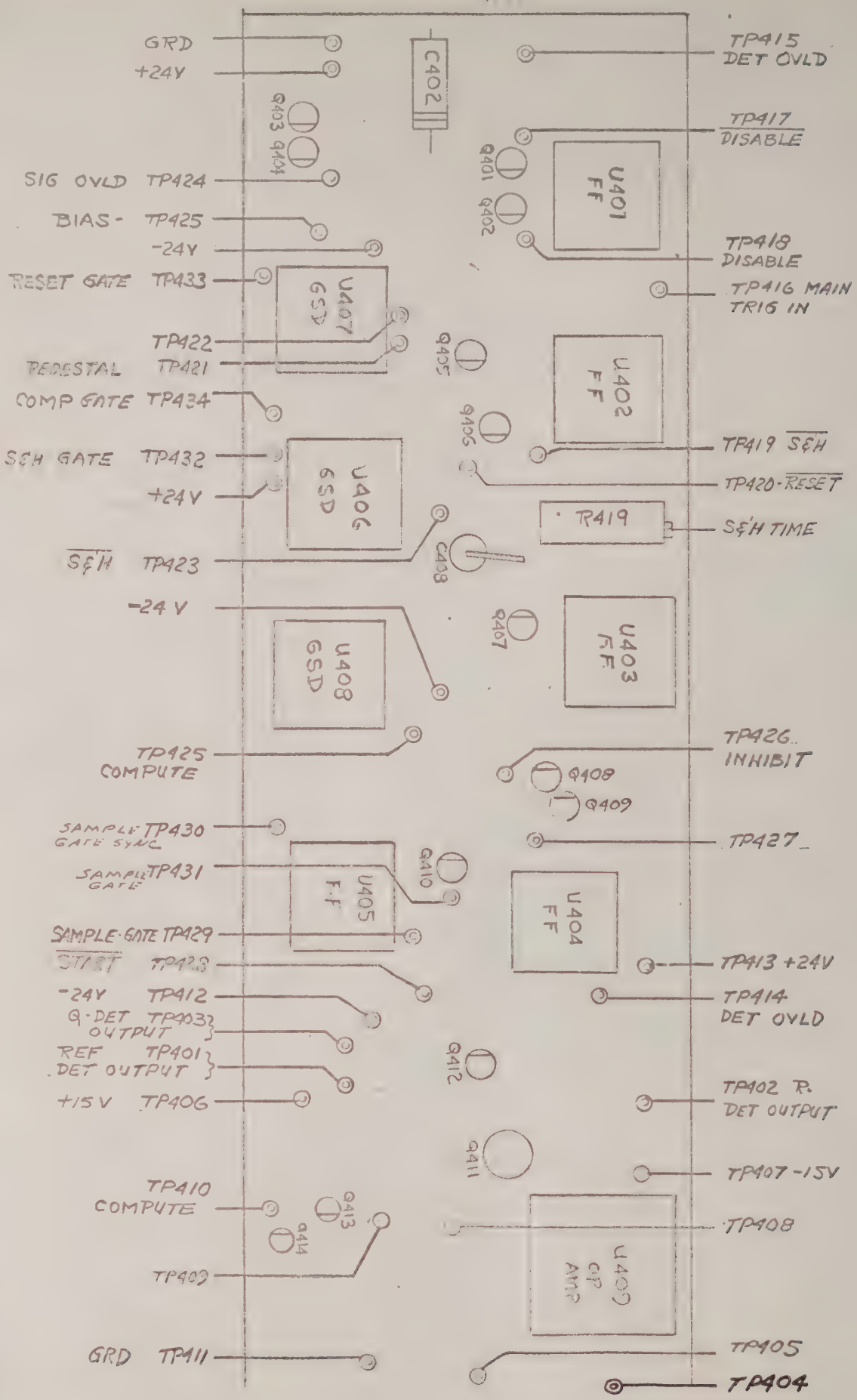
COMP ELEM CKT BOARD
XVIII
U310 OP AMPL
U309 SSS
U308 S.S.S
U307 VC
U306 VC
U305 SPI
U304 DSD
U303 ZCD
U302 VC
U301 VC
K301 RLY #1
K302 RLY #2
K303 RLY #3
C325
C323
C321
C319
C318
C317
C316
C315
C314
C313
C312
C311
C310
C309
C308
C307
C306
C305
C304
C303
C302
C301
R309
R314
R305
TP330 DETECTOR OUTPUT
TP319 -15V
TP318 +15V
BAL ADJ
TP310
TP312
TP311
M.F. ZERO ADJ
TP308
TP309
TP307
DETECTOR ZERO ADJ
ZCD BIAS ADJ
TP306
TP305 +20V
TP304 -20V
TP303
GRD TP321
SYNC SIG TP301
GRD TP322
INPUT SIG TP302
TP313
TP314
RESET GATE TP316
COMPUTE GATE TP317
TP315

FRONT END CKT BOARD
XIX
SIS 30MV (J801-6)
TP703
TP702
TP701
GND
3V REF (J801-9)
C701
U703 V-C
C702
U701 V-C
TP705
TP706
C703
TP708 INFO SIG
U702 V-C
TP707 REF SIG
C705
U704 V-C
C704
Q701
Q704
Q702
Q705
QUAD TP709 CKT DRIVE
REAL TP711 CH SYNC
C709
Q707
Q703
Q706
Q709
TP710 MAG SYNC
TP712
+20V
Q708
C711
C713
Q710
C712
C715
C714
C716
CKT GRD
+20V



XX

TIMING & OUTPUT CKT BOARD



XXI GATE CKT BOARD

INDEX OF ASSEMBLIES

Model 202 Serial Numbers 1 through 52

All Modules and Assemblies Suffixed Rev. A

Model 202 Serial Numbers 53 and Greater (see Note for Serial #70 and greater)

Front end circuits, assy 100756 B	Qty. 1	
Modules: V-C Ampl 100717 B	Qty. 4	
AC limit circuits, assy 100753B	Qty. 1	
Modules: F-F 100720	Qty. 4	
Computing Element:		
assy 100738B	Qty. 3	
Modules: SPI 100723A	Qty. 1	Per Assy
V-C Ampl 100717B	Qty. 4	" "
ZCD 100735B	Qty. 1	" "
DSD 100726B	Qty. 1	" "
SSS 100729A	Qty. 2	" "
Oper. Ampl. #210 Analog Dev.	Qty. 1	" "
Gate Circuits: Assy 100741B	Qty. 1	
Modules: F-F 100720B	Qty. 5	
GSD 100732A	Qty. 1	
Oper. Ampl. Nexus Sq. -10A	Qty. 1	
Timing & Output circuits: Assy 100747B		
Modules: F-F 100720B	Qty. 1	
SSS 100729 A	Qty. 1	
S&H 100775A	Qty. 2	
Quad. Circuit: Assy 100750B	Qty. 1	
Sig. Circuits Power Supply: Assy 100759B	Qty. 1	
SW & AUX Circuits Power Supply: Assy 100761B	Qty. 1	
Main Frame: Assy 100699B	Qty. 1	
Modules: L.F. 100774A	Qty. 1	
Bridging Unit: Assy 100713B	Qty. 1	(See Note)
Plug-In 202 Par 2501	Qty. 1	
Power E.F. Assy B100256	Qty. 1	

NOTE: Bridging Units Rev. A must be modified by the removal of two wires for use with Model 202 (A) Serial #70 and greater (See Schematic 100710 Rev. B). Rev. B Bridging Units may be used on all models.

Model 202A only

Coordinate converter Assy 101151	Qty. 1	

DWG NO. 100719 A

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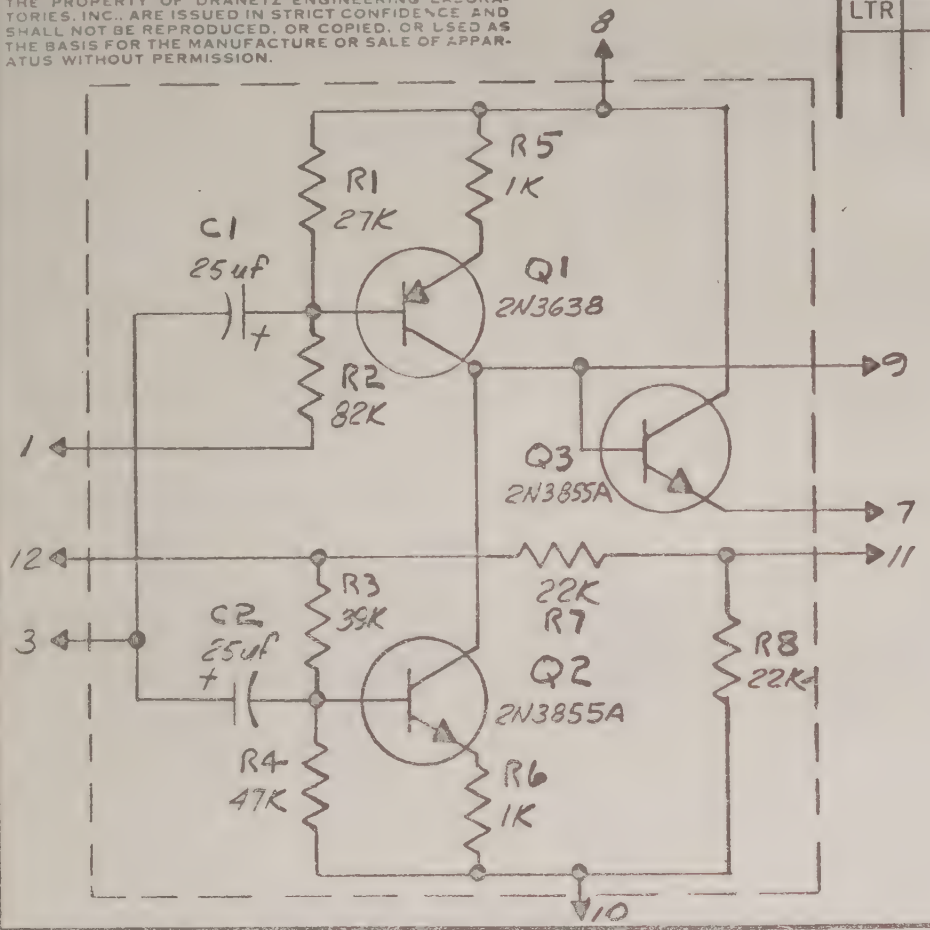
A ORIGINAL ISSUE	REVISIONS		
LTR	DESCRIPTION	DATE	APPROVED



PIN	FUNCTION
1	GRD
2	BLANK
3	INPUT
4	BLANK
5	BLANK
6	BLANK
7	VOLTAGE OUTPUT ← TRIM
8	+24V
9	CURRENT OUTPUT
10	-24V
11	TRIM (NOMINAL TO PIN 7)
12	EXT CAP (.25MA TO GRD)

1. 100717A, 5K INTERNALLY MOUNTED FROM PIN 1 TO PIN 9
2. REV A + B NOT INTERCHANGABLE

GROUP	NEXT ASSY	USED ON DS
G	—	202
G		
G		
G		
G		
G1		
	APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN Jm Barber 2/24/68
CKD
APPD [illegible] 3/4/68
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
V/C AMPL 100717B

SIZE	CODE IDENT. NO.		
A	23207	100719	A
		SHEET	

...ROLS CORP BROOKLYN, N.Y. 11217 REPRODUCED NO 440M

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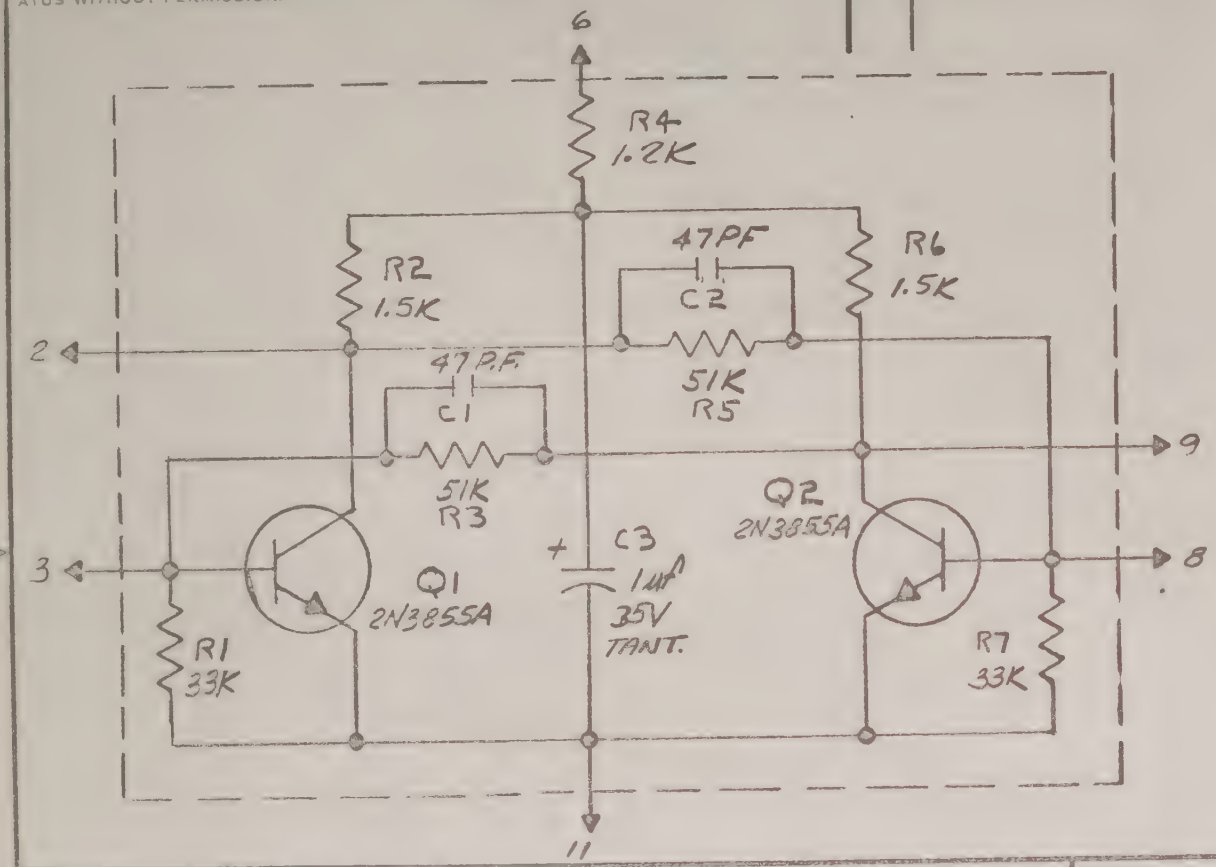
NO. 100722 A

REVISIONS			
A ORIGINAL ISSUE			
LTR	DESCRIPTION	DATE	APPROVED



PIN	FUNCTION
1	BLANK
2	OUTPUT J
3	INPUT J
4	BLANK
5	BLANK
6	+24 V
7	BLANK
8	INPUT K
9	OUTPUT K
10	BLANK
11	GRD

1. 100720A, C1 + C2 = 100 PF
2. REV A + B NOT INTERCHANGABLE

GROUP	NEXT ASSY	USED ON DS
G	—	202
G	—	215
G		
G		
G		
G		
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN J. M. Barber 2/24/68
CKD
APPD A. Vitale 3/4/68
DEL.

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
F-F 100720B

SIZE	CODE IDENT. NO.		
A	23207	100722	A
		SHEET	

GRAPHIC CONTROLS CORP., BROOKLYN, N. Y. 217 PEPPOVEL NO 440M

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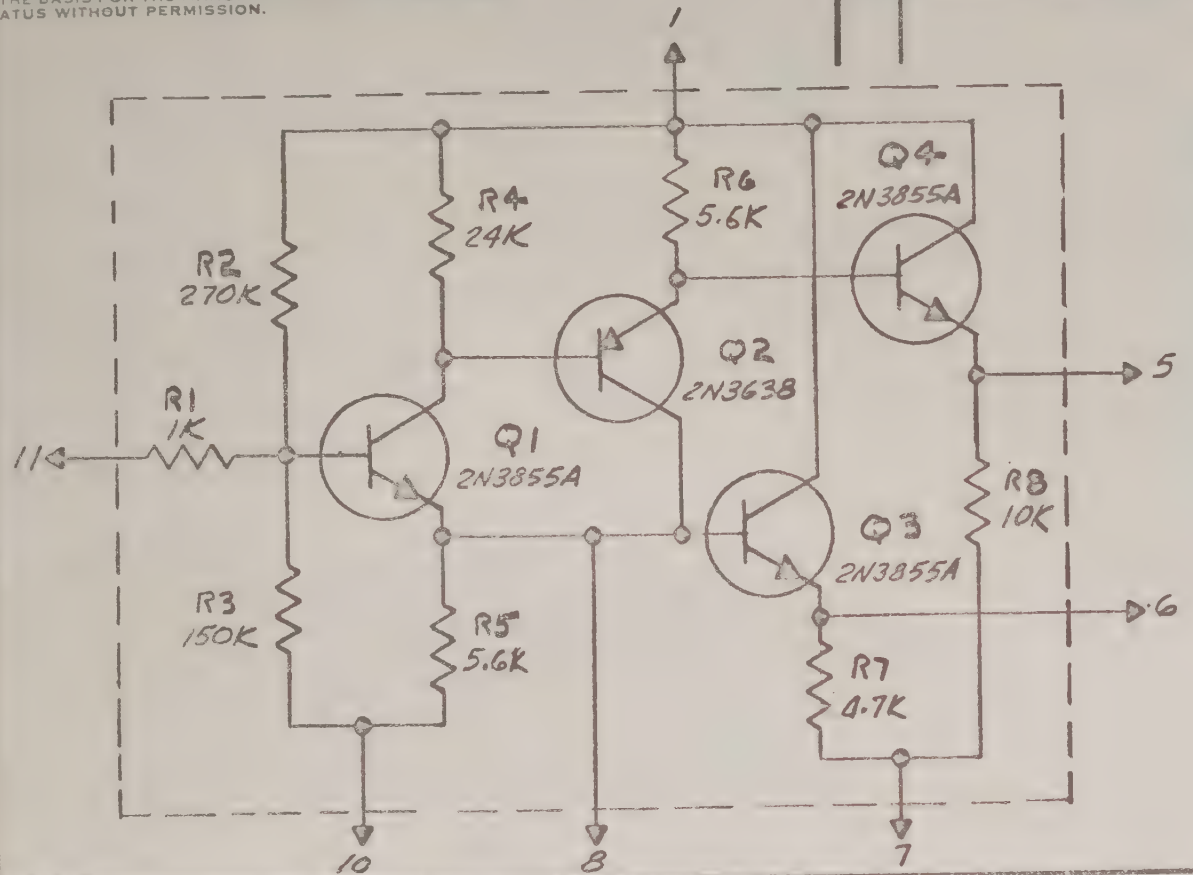
DWG NO. 100723 A

REVISIONS			
A ORIGINAL ISSUE			
LTR	DESCRIPTION	DATE	APPROVED



PIN	FUNCTION
1	+24V
2	BLANK
3	BLANK
4	BLANK
5	INVERTED OUTPUT
6	IN-PHASE OUTPUT
7	GRD
8	TRIM (NOM 24K TO GRD)
9	BLANK
10	GRD
11	INPUT (THRU .25MF)

GROUP	NEXT ASSY	USED ON DS
G	—	202
G	—	215
G		
G		
G		
G1		
	APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN Jim Barber 2/21/68
CKD
APPD 3/4/68
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
S.P.I. 100723A

SIZE	CODE IDENT NO.		
A	23207	100725	A
		SHEET	

PAPMIC CONTROLS CORP. BROOKLYN N Y 11217 REPROVEL NO 440M

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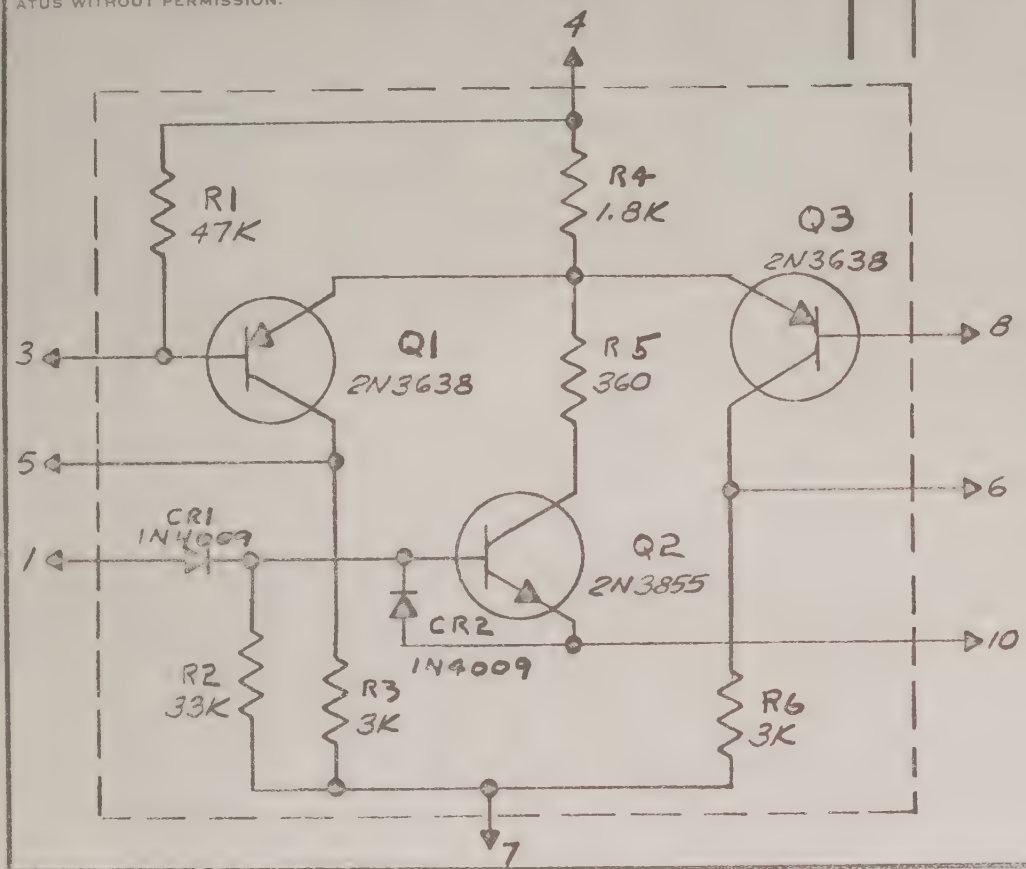
DWG NO. 100728 A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL ISSUE		



PIN	FUNCTION
1	SAMPLE GATE INPUT
2	BLANK
3	SYNC INPUT
4	+24V
5	OUTPUT #1
6	OUTPUT #2
7	-24V
8	BIAS (+5.5V)
9	BLANK
10	GRD
11	BLANK

1. 100726A, R1 NOT USED
2. REV B DIRECT REPLACEMENT FOR REV A

GROUP	NEXT ASSY	USED ON DS
	APPLICATION	

202

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± 005

CONTR
DWN Jim Bertier 2/21/68
CKD
APPD
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
D.S.D. 100726B

SIZE	CODE IDENT. NO.	100728	A
A	23207		

SHEET

GRAPHIC CONTROLS CORP BROOKLYN, N Y 11217 REPROVEL NO. 440M

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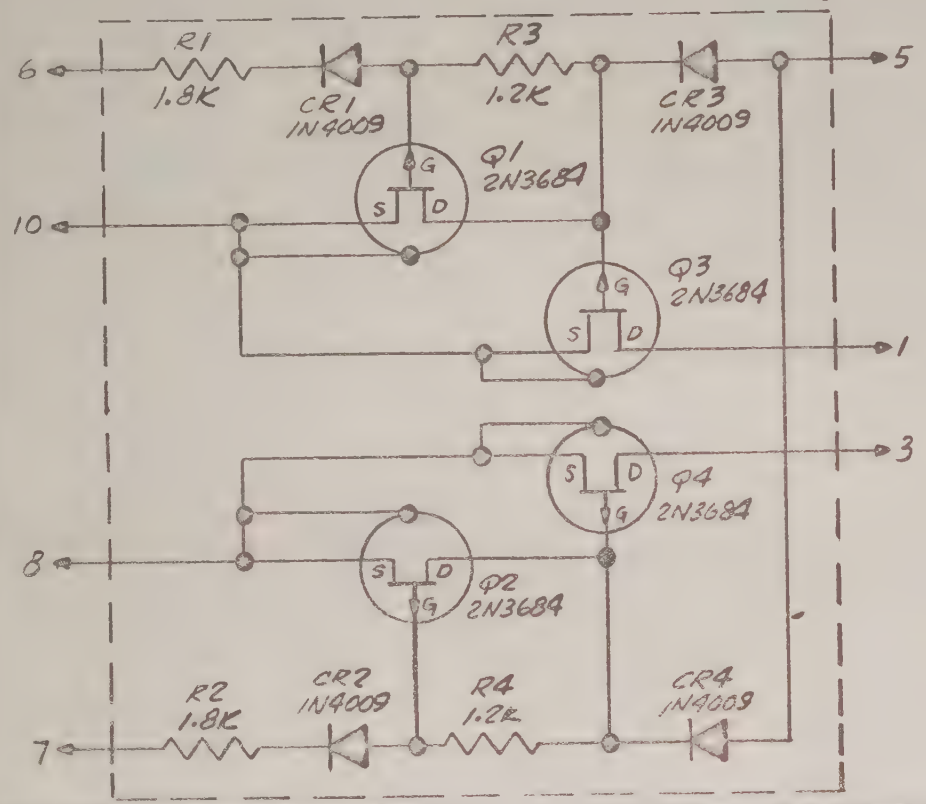
DWG NO.

REVISIONS			
A ORIGINAL ISSUE			
LTR	DESCRIPTION	DATE	APPROVED



PIN	FUNCTION
1	OUTPUT SWITCH #1
2	BLANK
3	OUTPUT SWITCH #2
4	BLANK
5	REF (-8V OR -15V
6	GATE SWITCH #1
7	GATE SWITCH #2
8	INPUT SWITCH #2
9	BLANK
10	INPUT SWITCH #1
11	BLANK

GROUP	NEXT ASSY	USED ON DS
G	—	202
G	—	215
G		
G		
G		
G1		
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN J. Barber 3/6/68
CKD
APPD
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
S. S. S. (100729A)

SIZE	CODE IDENT NO.		REV
A	23207	100731	A
		SHEET	

GRAPHIC CONTROLS CORP., BROOKLYN, N. Y. 11217 REPROVEL NO. 440M

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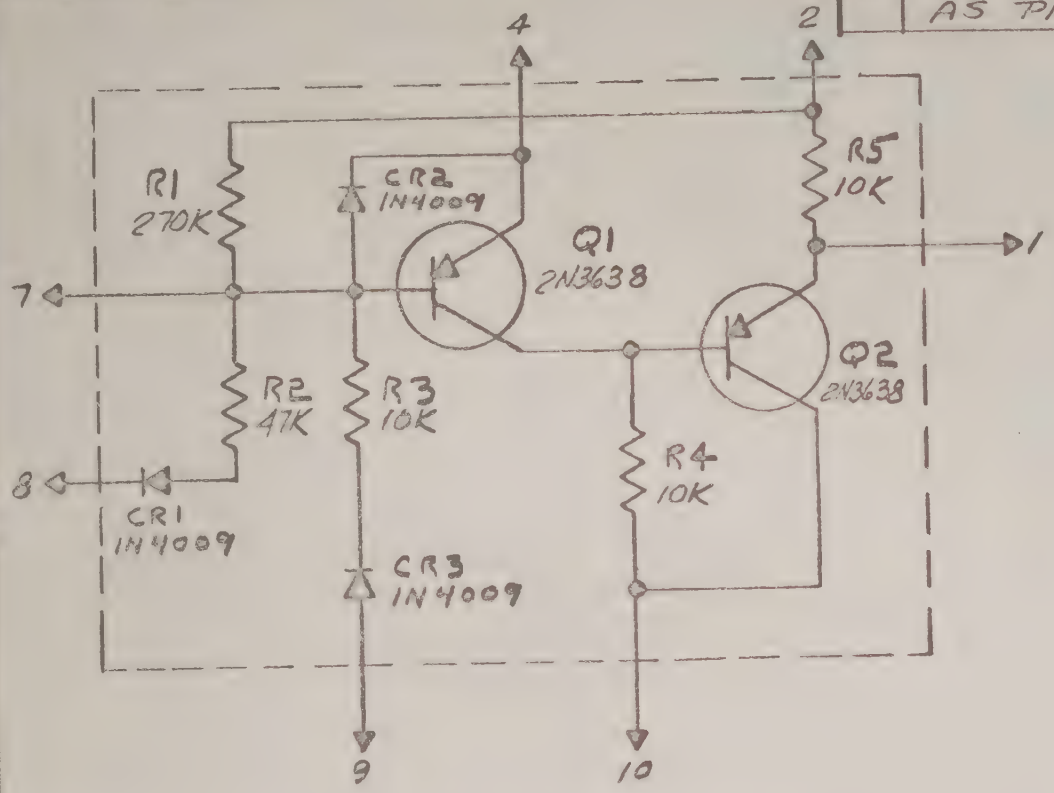
DWG NO. 100734 B

REVISIONS			
A ORIGINAL ISSUE			
LTR	DESCRIPTION	DATE	APPROVED
B	GATE OUTPUT WAS INDICATED AS PIN #11	6-3-68	GT



PIN	FUNCTION
1	GATE OUTPUT
2	+24V
3	BLANK
4	BIAS +7V NOM
5	BLANK
6	BLANK
7	AUX INPUT
8	INPUT
9	INHIBIT
10	-24V
11	BLANK

GROUP		
G	—	202
G		
G		
G		
G		
G1		
NEXT ASSY		USED ON DS
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN Jim Barber 2/14/68
CKD
APPD
DEL

DRANETZ ENGINEERING LABORATORIES INC.
PLAINFIELD NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
G.S.D. 1,00732A

SIZE	CODE IDENT NO.		
A	23207	100734	B
		SHEET	

GRAPHIC CONTROLS CORP., BROOKLYN, N.Y. 11217 REPROVEL NO. 440M

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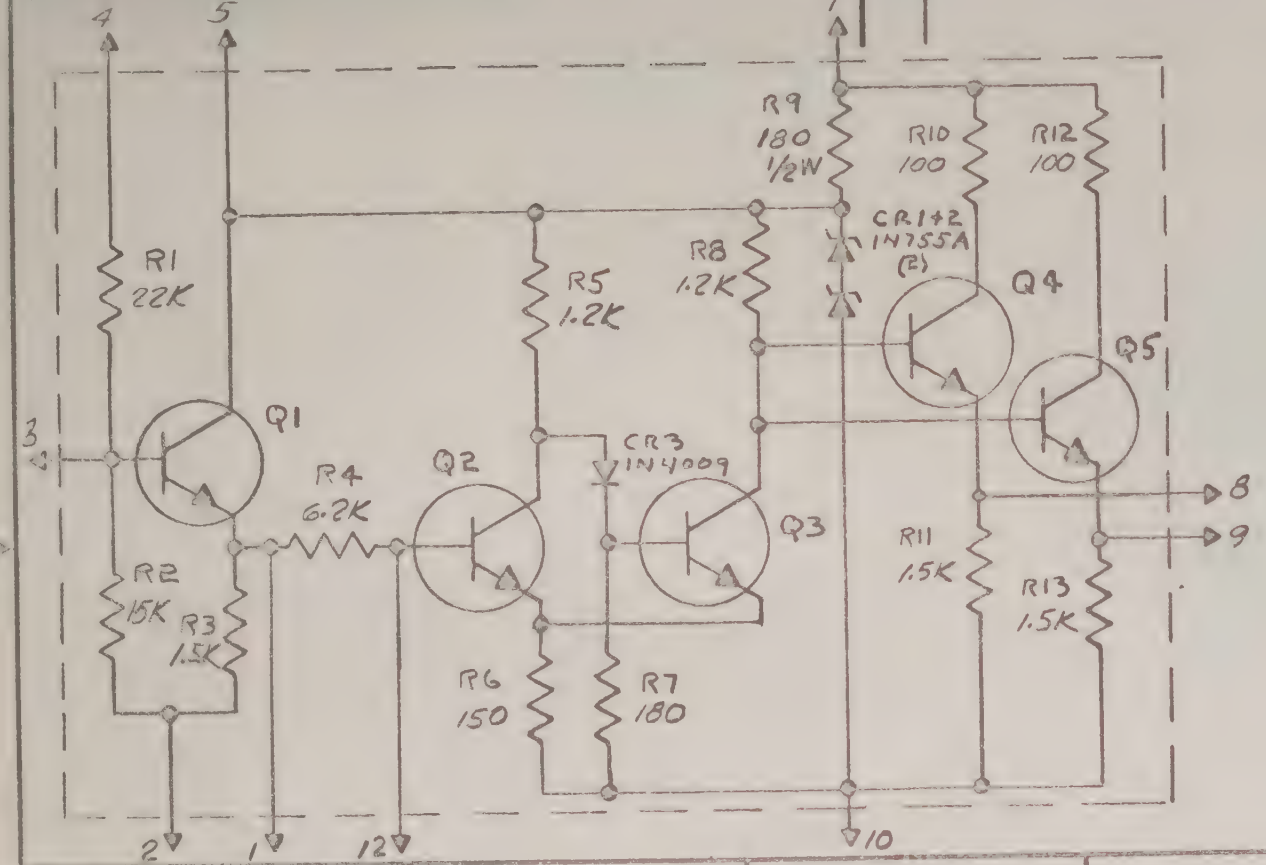
NO.

REVISIONS			
A ORIGINAL ISSUE			
LTR	DESCRIPTION	DATE	APPROVED



PIN	FUNCTION
1	TRIM (420 PF TO 12)
2	GRD
3	INPUT (THRU 20MΩ)
4	TRIM (100K POT TO 5)
5	+15V
6	BLANK
7	+24V
8	OUTPUT
9	OUTPUT
10	GRD
11	BLANK
12	TRIM SEE 1 ABOVE

1. 100735A, R11 + R13 ARE 5.1K
2. ALL TRANSISTORS 2N3855A
3. REV A + B NOT INTER-CHANGABLE

GROUP	NEXT ASSY	USED ON DS
G	—	202
G	—	215
G		
G		
G		
G1		
	APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN J. Barber 2/24/68
CKD
APPD 3/4/68
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
Z.C.D. 100735B

SIZE	CODE IDENT. NO.		
A	23207	100737	A
		SHEET	

GRAPHIC CONTROLS CORP., BROOKLYN, N. Y. 11217 REPROVEL NO. 440M

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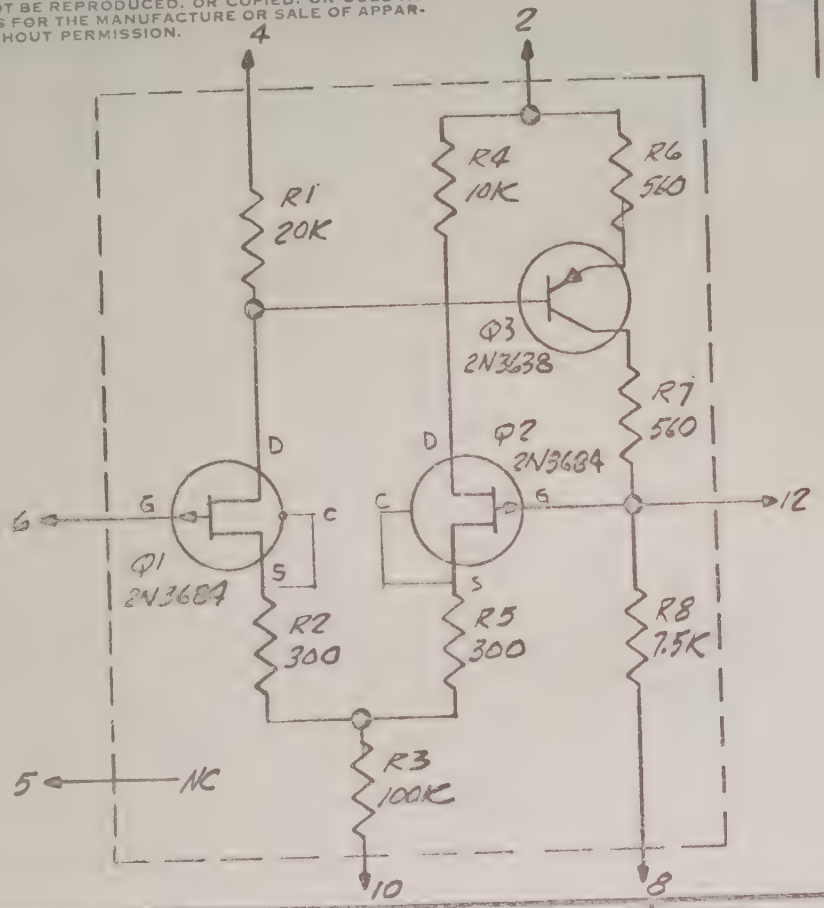
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL ISSUE		



PIN	FUNCTION
1	BLANK
2	+24V
3	BLANK
4	ZERO ADJ (100K POT TO +24V
5	POLARIZING PIN
6	INPUT
7	BLANK
8	-24V
9	BLANK
10	TRIM (100K POT TO -24V
11	BLANK
12	OUTPUT

GROUP	NEXT ASSY	USED ON DS
G		202
G		215
G		
G		
G		
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN Jon Sauber 3/6/68
CKD
APPD
DEL

DRANETZ ENGINEERING LABORATORIES INC.
PLAINFIELD NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM S&H (100775A)

SIZE	CODE IDENT NO.		REV
A	23207	100882	A

SHEET

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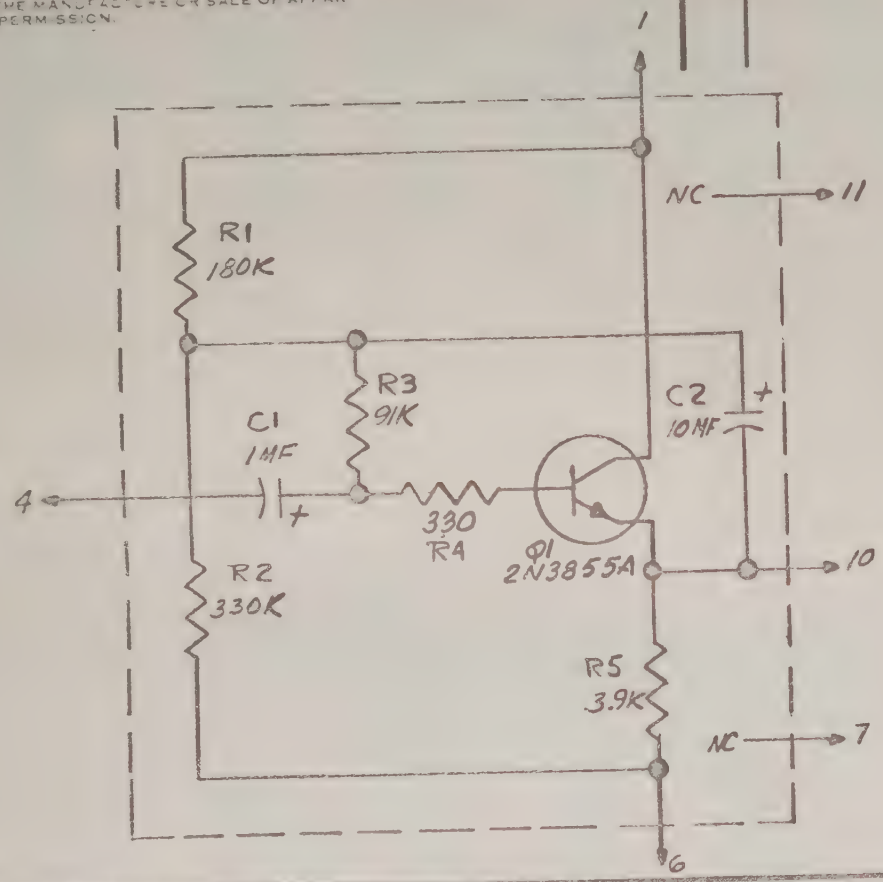
DWG NO.

LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL ISSUE		

REVISIONS



PIN	FUNCTION
1	+24V
2	BLANK
3	BLANK
4	INPUT
5	BLANK
6	-24V
7	POLARIZING PIN
8	BLANK
9	BLANK
10	OUTPUT
11	POLARIZING PIN

G	—	202
G		
G		
G		
G		
S1		
GROUP	NEXT ASSY	USED ON
	APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
COML. TOL. APPLY TO STOCK SIZES
FRACTION ± 1/64
3 PLACE ± .005

CONTR
DWN J. Barber 3/4/68
CKD
APPD
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
E.F. (100774A)

SIZE	CODE IDENT. NO.		REV
A	23207	100883	A
		SHEET	

GRAPHIC CONTROLS CORP., BROOKLYN, N.Y. 11213 FORM NO. 44M

PIN	FRONT PANEL CONNECTORS (MATES WITH P101) CONN. 1A	AC LIMITS CIRCUIT (100753) CONN. 2A	(X CHANNEL) COMPUTING ELEMENT (100738) CONN. 3A	(R CHANNEL) COMPUTING ELEMENT (100738) CONN. 4A	(Y CHANNEL) COMPUTING ELEMENT (100738) CONN. 5A	GATE CIRCUITS (100741) CONN. 6A	TIMING & OUTPUT CIRCUITS (100747) CONN. 7A	AUX CIRCUITS (Z-Ø CONVERTER) (OPTIONAL) CONN. 8A
1	X CH SYNC	X CH SYNC	X CH SYNC	R CH SYNC	REF CH SYNC		GO LIGHT	
2	REF CH SYNC	REF CH SYNC	X CH SYNC	R CH SIGNAL	REF CH SIGNAL		OUT OF LIMITS	OUT OF LIMITS
3	R CH SYNC	GRD	GRD	GRD	GRD	GRD	GRD	GRD
4	REF CH SIGNAL	GRD	GRD	GRD	GRD	GRD	GRD	GRD
5	FS MAG POT	MAIN TRIGGER	MAIN TRIGGER	MAIN TRIGGER	MAIN TRIGGER	MAIN TRIGGER	DISABLE OUTPUT	DISABLE OUTPUT
6	GRD	GRD	GRD	GRD	GRD	DISABLE	DISABLE	
7	GRD	GRD	GRD	GRD	GRD		RESET OUTPUT	RESET OUTPUT
8	GRD	SIGNAL GUILD	SIGNAL GUILD	SIGNAL GUILD	SIGNAL GUILD	SIGNAL GUILD	MARK OUTPUT	MARK OUTPUT
9	X CH SIGNAL	PEDESTAL	PEDESTAL	PEDESTAL	PEDESTAL	PEDESTAL	PEDESTAL	
10	-20V	-20V	+18V	+18V	+18V		QUAD ZERO	Z OUTPUT
11	+20V	+20V	-18V	-18V	-18V	S & H GATE	S & H GATE	Ø OUTPUT
12	MAG SYNC	MAG SYNC					REC SEEK	REC SEEK
13	FS SAL POT					HOLD	HOLD	
14		+24V	+24V	+24V	+24V	+24V	+24V	+24V
15	R CH SIGNAL	-24V	-24V	-24V	-24V	-24V	-24V	-24V

PIN	(MATES WITH P102) CONN. 1B	CONN. 2B	CONN. 3B	CONN. 4B	CONN. 5B	CONN. 6B	CONN. 7B	CONN. 8B
1		AC SIGNAL OUTPUT			SAMPLE GATE SYNC	SAMPLE GATE	SYNC	
2		AC REF OUTPUT	RESET GATE	RESET GATE	RESET GATE	RESET GATE		
3		REF LEVEL IND	COMPUTE GATE	COMPUTE GATE	COMPUTE GATE	COMPUTE GATE		
4			SAMPLE GATE	SAMPLE GATE	SAMPLE GATE	SAMPLE GATE		
5		SAMPLE INHIBIT	SAMPLE INHIBIT	SAMPLE INH.	SAMPLE INHIBIT	SAMPLE INHIBIT		
6				X CH LEVEL	X CH LEVEL	X CH LEVEL	Y CH LEVEL	
7					R CH LEVEL	R CH LEVEL	R CH LEVEL	
8			X CH LEVEL	R CH LEVEL	REF CH LEVEL	REF CH LEVEL	TRIGGER OUTPUT	TRIGGER OUTPUT
9	+36V	GRD	GRD	GRD	GRD	GRD	R SIGNAL OUTPUT	R SIGNAL OUTPUT
10		-15V	-15V	-15V	-15V	-15V	X SIGNAL OUTPUT	X SIGNAL OUTPUT
11		+15V	+15V	+15V	+15V	+15V	AUX TRIG	AUX TRIG
12	RELAY GRD	RELAY GRD	RELAY GRD	RELAY GRD	RELAY GRD		PULSE SWITCH	
13	RELAY #3	RELAY #3	RELAY #3	RELAY #3	RELAY #3		CW SWITCH	
14	RELAY #2	RELAY #2	RELAY #2	RELAY #2	RELAY #2	COMP LEVEL POT	TRIG LEVEL POT	TRIG LEVEL POT
15	RELAY #1	RELAY #1	RELAY #1	RELAY #1	RELAY #1	COMP LEVEL POT	TRIG LEVEL POT	TRIG LEVEL POT

CONTR
CONN. NO.
CKD BG
DWD

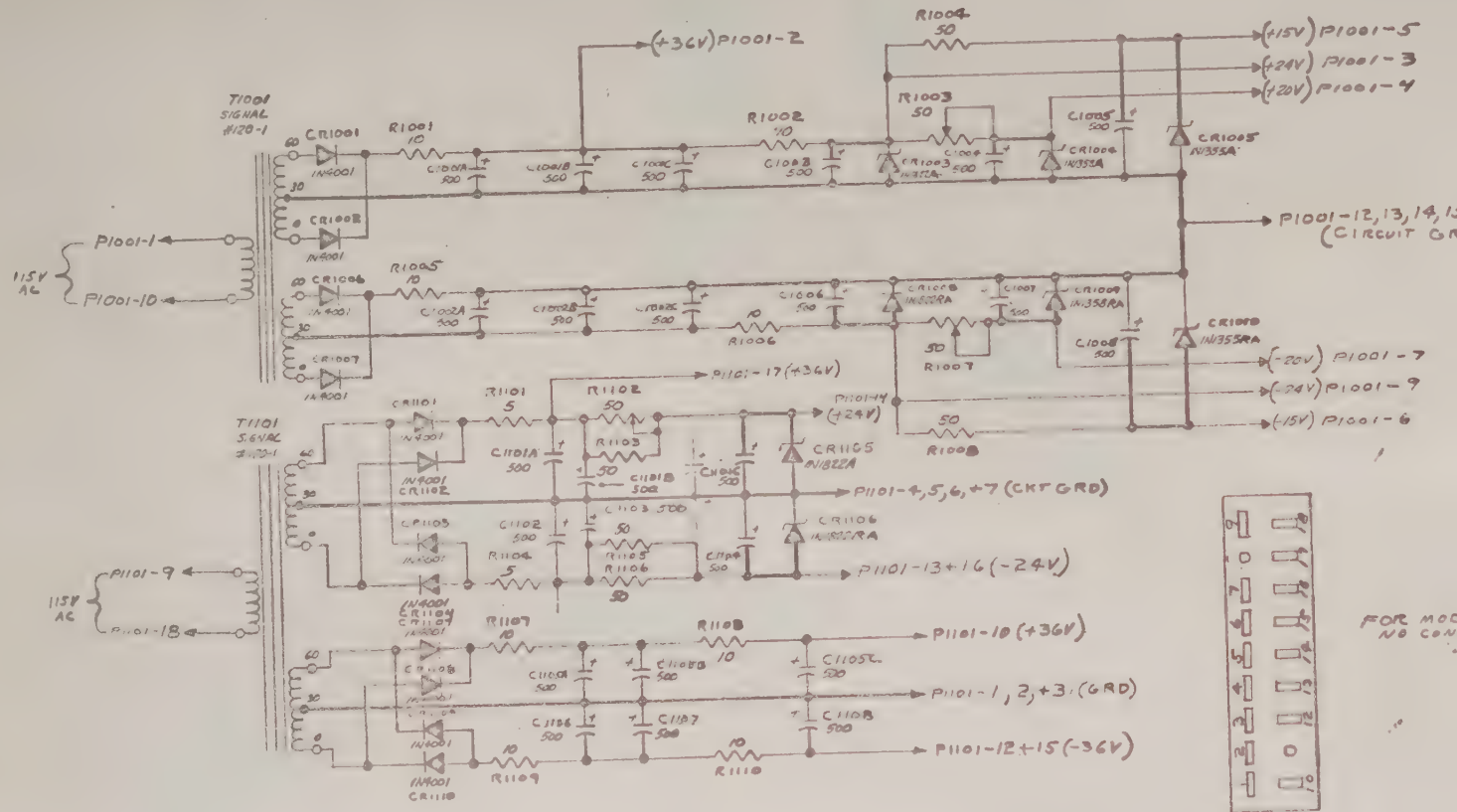
GRANETZ ENGR LABS PLAINFIELD N.J

CONNECTOR PIN FUNCTION CHART

100,746

SIZE		REV
B	100 746	A

SHEET 1 OF 1



FOR MODEL 202 S/U 1 THRU 5 NO CONNECTORS USED

FRONT VIEW P1001 + P1101

NOTES:
1. ALL RESISTORS ±10%, 10 WATT WIRE WOUND UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS IN MFD, 50VV
3. P1001 MATES WITH J804, P1101 MATES WITH J803

LIST OF MATERIALS

GI QTY	U M	ITEM	CODE IDENT	PART OR IDENTIFYING NO	DESCRIPTION

DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY USA

APPROVALS SIGNATURE & DATE

DRAWN	[illegible] 29 NOV 1967
CHECKED	
[illegible]	
[illegible]	
[illegible]	
[illegible]	

SCHEMATIC DIAGRAM
SIG CKTS P.S (100759B)
SW + AUX CKTS P.S (100760B)

SIZE C | CAGE CODE 23207 | 100763 | A

SCALE [illegible] | SHEET [illegible]

MATERIAL

FINISH

MARKING

DIMENSIONS ARE IN INCHES. TOLERANCES UNLESS OTHERWISE SPECIFIED: FRACTIONALS ±1/16, DECIMALS .X ±.1, .XX ±.02, .XXX ±.005, ANGULAR ±1°

4 IN PART NO. COL DENOTES VENDOR ITEM; SEE SOURCE CONTROL OR SPECIFICATION DRAWING.

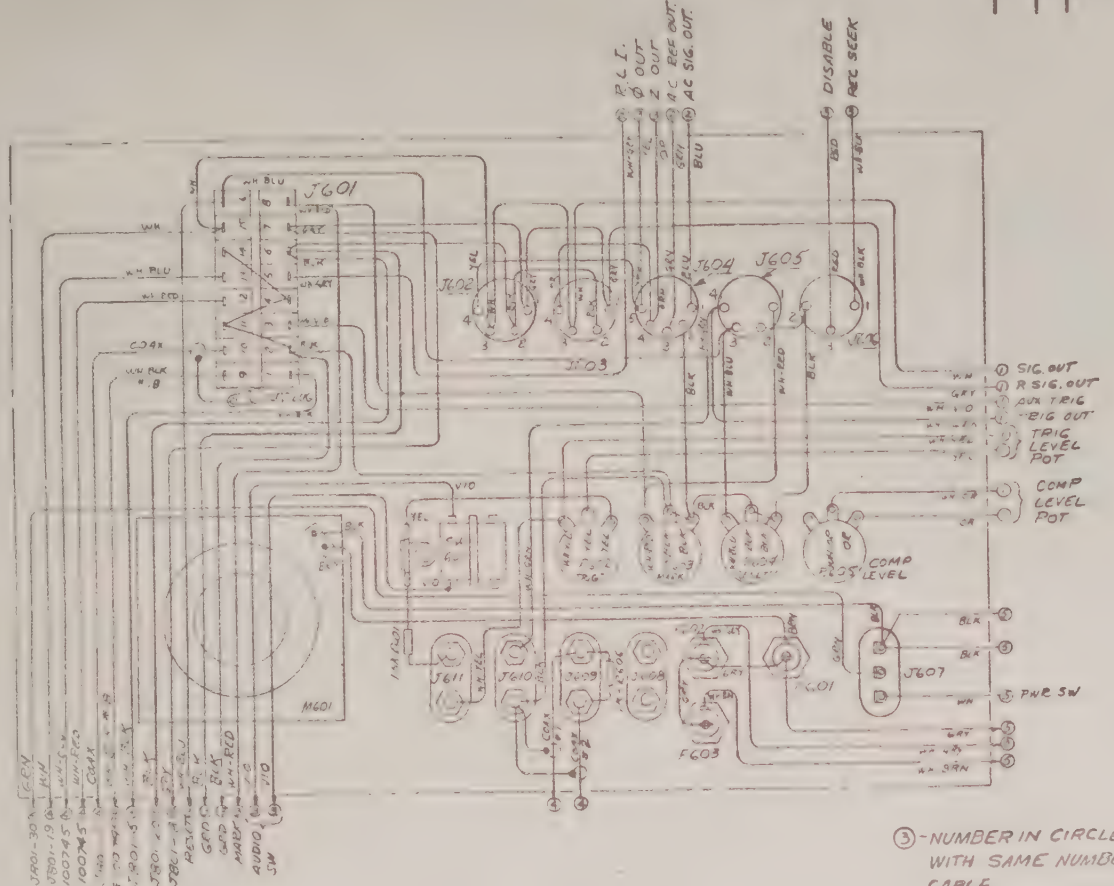
COML TOL APPLY TO STOCK SIZES

U OF M CODE | 1 PIECE 6 PAR 5 SET 32 FEET 54 U.S. LIQUID QT. 68 LB. AVDP

OTHER

REPRODUCTION OF THIS DRAWING IN WHOLE OR IN PART WITHOUT WRITTEN PERMISSION OF DRANETZ ENGINEERING LABORATORIES, INC. IS PROHIBITED.

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL ISSUE		



③-NUMBER IN CIRCLE INDICATES-THOSE WIRES WITH SAME NUMBER BREAK OUT OF SAME CABLE

GI QTY REQD	U/M	ITEM NO	SIZE	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

MATERIAL	
FINISH	
GROUP	USED ON APPLICATION

* IN PART NO. COL. DENOTES VENDOR ITEM. SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING.

DECIMAL DIMENSION	PLACE	ANGLE	FRACTIONS
6-24 INCL	± .03		
OVER 24	±		± 1/16

COML TOL APPLY TO STOCK SIZES

CONTRACT

APPROVALS SIGNATURE & DATE

DRAWN	J. Sawtelle 3-21-68
CHECKED	R. Gilmore 3-22-68
MECH	
ELECT	
ENGR	
DEL	
OTHER	

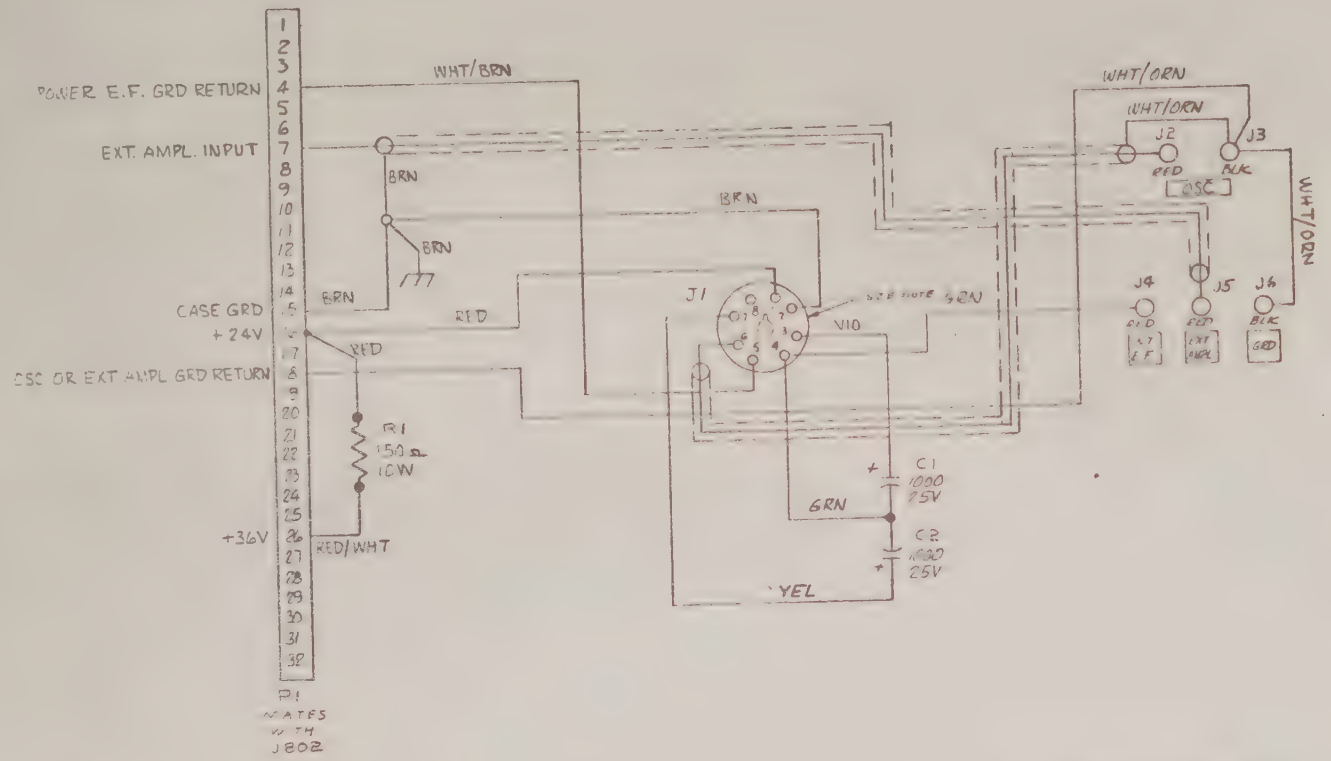
U OF M | PRICE GP | 1 OZ 55 U S GAL | 1 QT 68 LB. AVDP

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

REAR PANEL WIRING (MODEL 202)

SIZE	DRAWING NO.	REV
C	23207	

SCALE | SHT 1 OF 2



ZONE	LTR	REVISIONS: DESCRIPTION	DATE	APPROVED
	A	ORIGINAL ISSUE		

1 ASSEMBLY 100256 SEE SCHEMATIC 100247

LIST OF MATERIALS

QTY	ITEM NO	SIZE	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SEL SOURCE

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

SCHEMATIC DIAGRAM
POWER EMITTER FOLLOWER PLUG-IN
MODEL 202-PA-2501

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	23207	100705	A

SCALE — SHEET

APPROVALS SIGNATURE & DATE
DRAWN Jorgenson 11 DEC. 1967
CHECKED
ENGR
SELECT
STDS
QUAL
OTHER

CONTRACT

MATERIAL
FINISH
APPLICATION
202

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE AS FOLLOWS

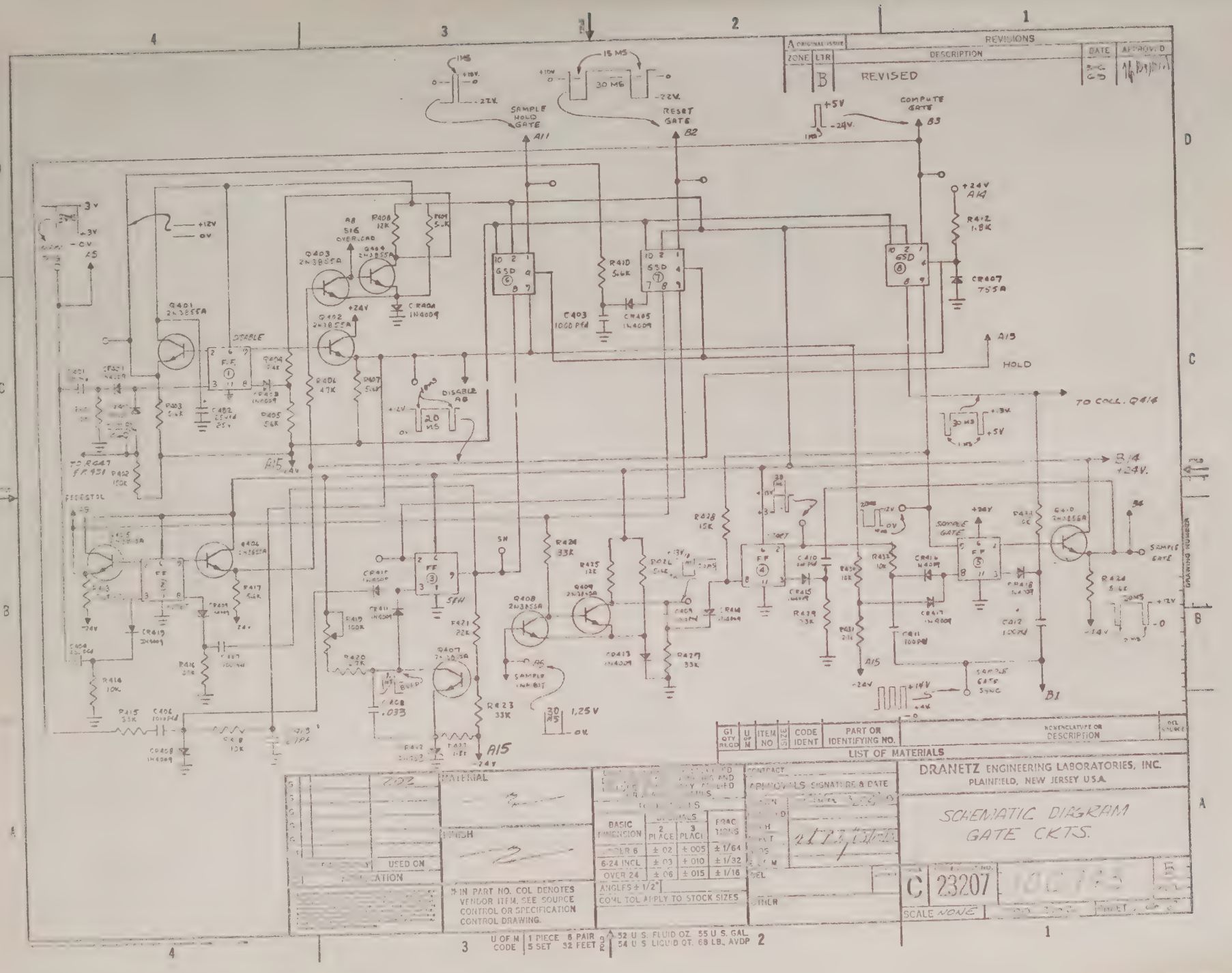
BASIC DIMENSION	DECIMALS 2 PLACE	DECIMALS 3 PLACE	FRACTIONS
UNDER 6	± .02	± .005	± 1/64
6 24 INCL	± .03	± .010	± 1/32
OVER 24	± .06	± .015	± 1/16
ANGLES ± 1/2°			

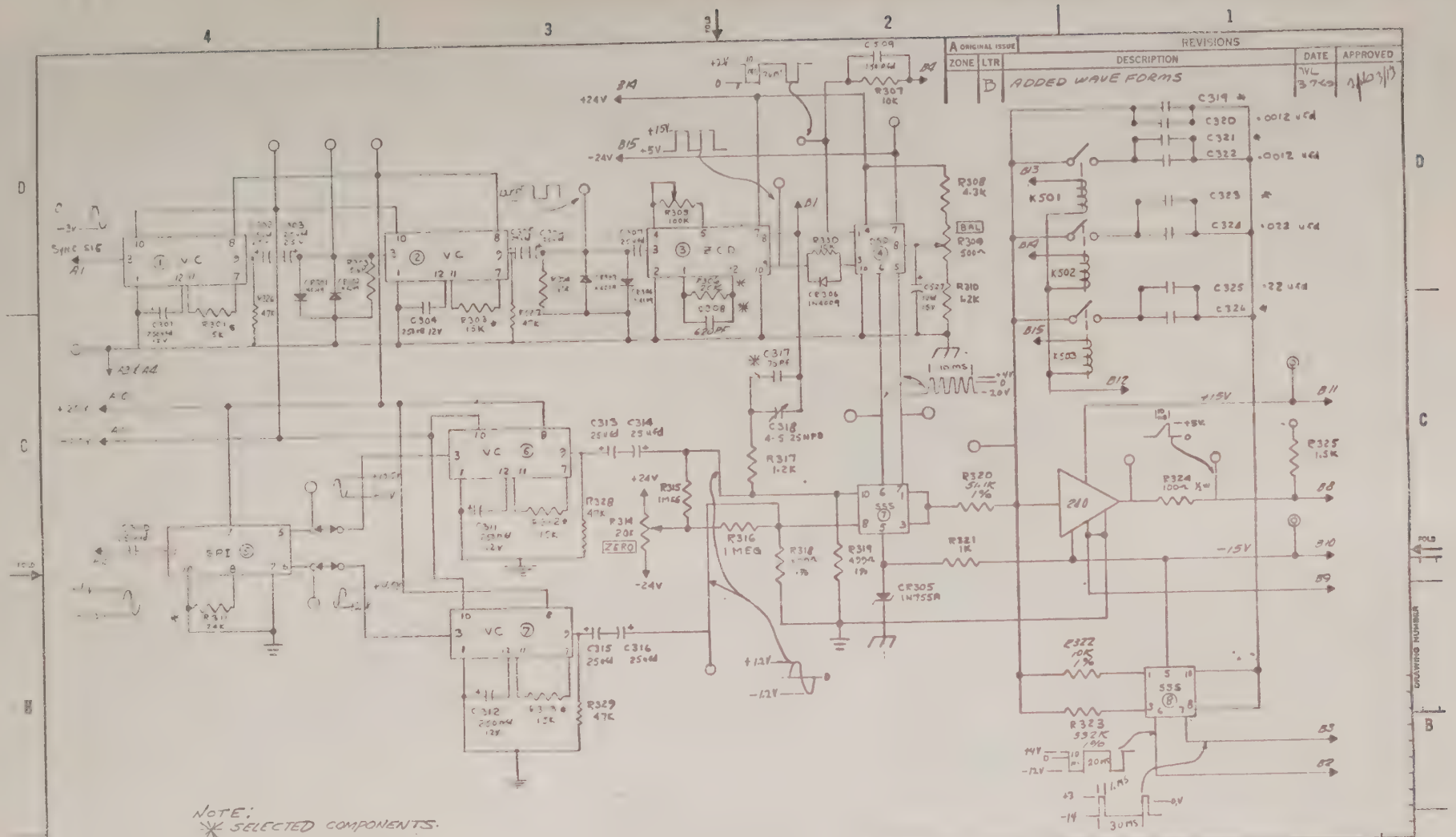
COML TOL APPLY TO STOCK SIZES

* IN PART NO. COL DENOTES VENDOR ITEM; SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING.

U OF M CODE | 1 PIECE 6 PAIR 5 SET 32 FEET | 52 U S FLUID OZ 55 U S GAL 14 U S L 3.4 AMOS

DRAWING NUMBER 100705 A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B | REVISED
SAMPLE HOLD GATE
RESET GATE
COMPUTE GATE
+24V
-24V
+12V
0V
+5V
-22V
+10V
1MS
15 MS
30 MS
20 MS
Q401 2N3855A
Q402 2N3855A
Q403 2N3855A
Q404 2N3855A
Q405 2N3855A
Q406 2N3855A
Q407 2N3855A
Q408 2N3855A
Q409 2N3855A
Q410 2N3855A
F.F. 1
F.F. 2
F.F. 3
F.F. 4
F.F. 5
GSD 6
GSD 7
GSD 8
DISABLE
DISABLE AB
HOLD
TO COLL. Q414
SAMPLE GATE
SAMPLE GATE SYNC
SAMPLE INHIBIT
1.25V
FEEDBTOL
TO R447 FR431
R401 5K
R402 150K
R403 5K
R404 5K
R405 5K
R406 47K
R407 5K
R408 12K
R409 5K
R410 5.6K
R411 47K
R412 1.8K
R413 5K
R414 10K
R415 33K
R416 10K
R417 5.6K
R418 100K
R419 100K
R420 2K
R421 22K
R422 33K
R423 33K
R424 33K
R425 12K
R426 5.6K
R427 33K
R428 15K
R429 33K
R430 10K
R431 10K
R432 2K
R433 10K
R434 5.6K
C401 .01 MFD
C402 100 MFD 25V
C403 1000 PFD
C404 .033
C405 100 PFD
C406 100 PFD
C407 100 PFD
C408 .033
C409 .01 MFD
C410 100 PFD
C411 100 PFD
C412 1000 PFD
CR401 IN4009
CR402 IN4009
CR403 IN4009
CR404 IN4009
CR405 IN4009
CR406 IN4009
CR407 755A
CR408 IN4009
CR409 IN4009
CR410 IN4009
CR411 IN4009
CR412 IN4009
CR413 IN4009
CR414 IN4009
CR415 IN4009
CR416 IN4009
CR417 IN4009
CR418 IN4009
CR419 IN4009
CR420 IN4009
CR421 IN4009
CR422 IN4009
A15
A11
B2
B3
A14
B14
B1
A5
SH
SFH
LIST OF MATERIALS
GI QTY REQD | U OF M | ITEM NO | SYM | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | CCL LTR/REV
DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.
SCHEMATIC DIAGRAM
GATE CKTS.
C | 23207
SCALE NONE
MATERIAL
FINISH
USED ON
* IN PART NO. COL DENOTES VENDOR ITEM, SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING.
BASIC DIMENSION | 2 PLACE | 3 PLACES | FRACTIONS
OVER 6 | ± .02 | ± .005 | ± 1/64
6-24 INCL | ± .03 | ± .010 | ± 1/32
OVER 24 | ± .06 | ± .015 | ± 1/16
ANGLES ± 1/2°
COML TOL APPLY TO STOCK SIZES
U OF M CODE | 1 PIECE 6 PAIR 52 U.S. FLUID OZ. 55 U.S. GAL. | 5 SET 32 FEET 54 U.S. LIQUID QT. 68 LB. AVDP



GI QTY REQD	U OF M	ITEM NO	SCH	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CEI SOURCE

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES

BASIC DIMENSION	DECIMALS 2 PLACE	DECIMALS 3 PLACE	FRACTIONS
UNDER 6	± .02	± .005	± 1/64
6-24 INCL	± .03	± .010	± 1/32
OVER 24	± .06	± .015	± 1/16

ANGLES ± 1/2°
COML TOL APPLY TO STOCK SIZES

CONTRACT

APPROVALS SIGNATURE & DATE

DRAWN 3/7/68
CHECKED
MECH
ELECT
DEL

DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

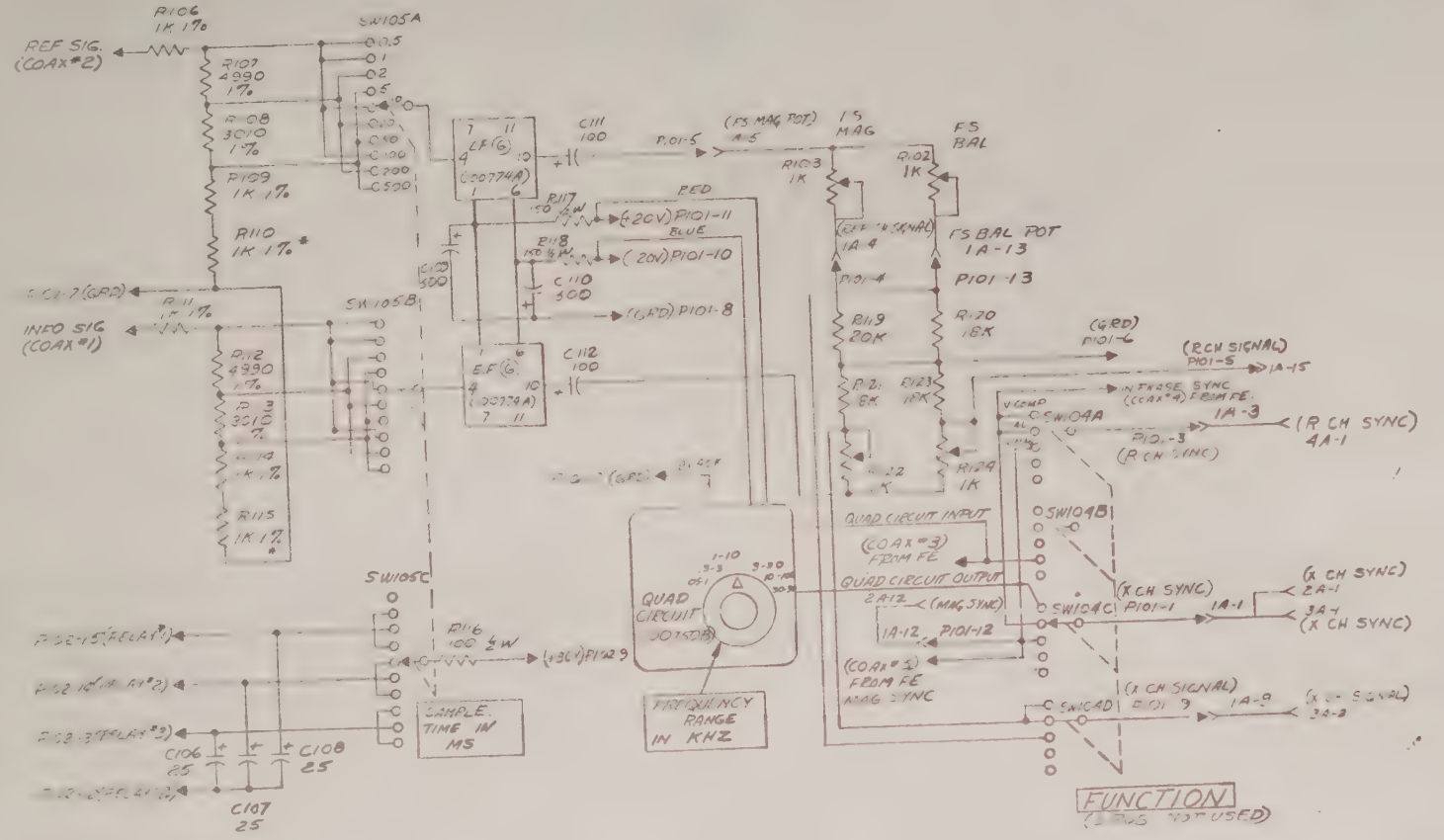
SCHEMATIC DIAGRAM
COMP ELEM

SIZE C | CODE IDENT NO. 23207 | DRAWING NUMBER

SCALE NONE | SHEET

202

1 PIECE 6 PAIR 5 SET 32 FEET | 55 U.S. GAL



ITEM	U/M	ITEM NO	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CEL SOURCE

LIST OF MATERIALS

DRANETZ ENGINEERING LABORATORIES INC
PLAINFIELD NEW JERSEY U.S.A.

SCHEMATIC
FRONT PANEL

SIZE	CAGE NO	DRAWING NO	REV
C	23207	100884	A

SCALE

MATERIAL

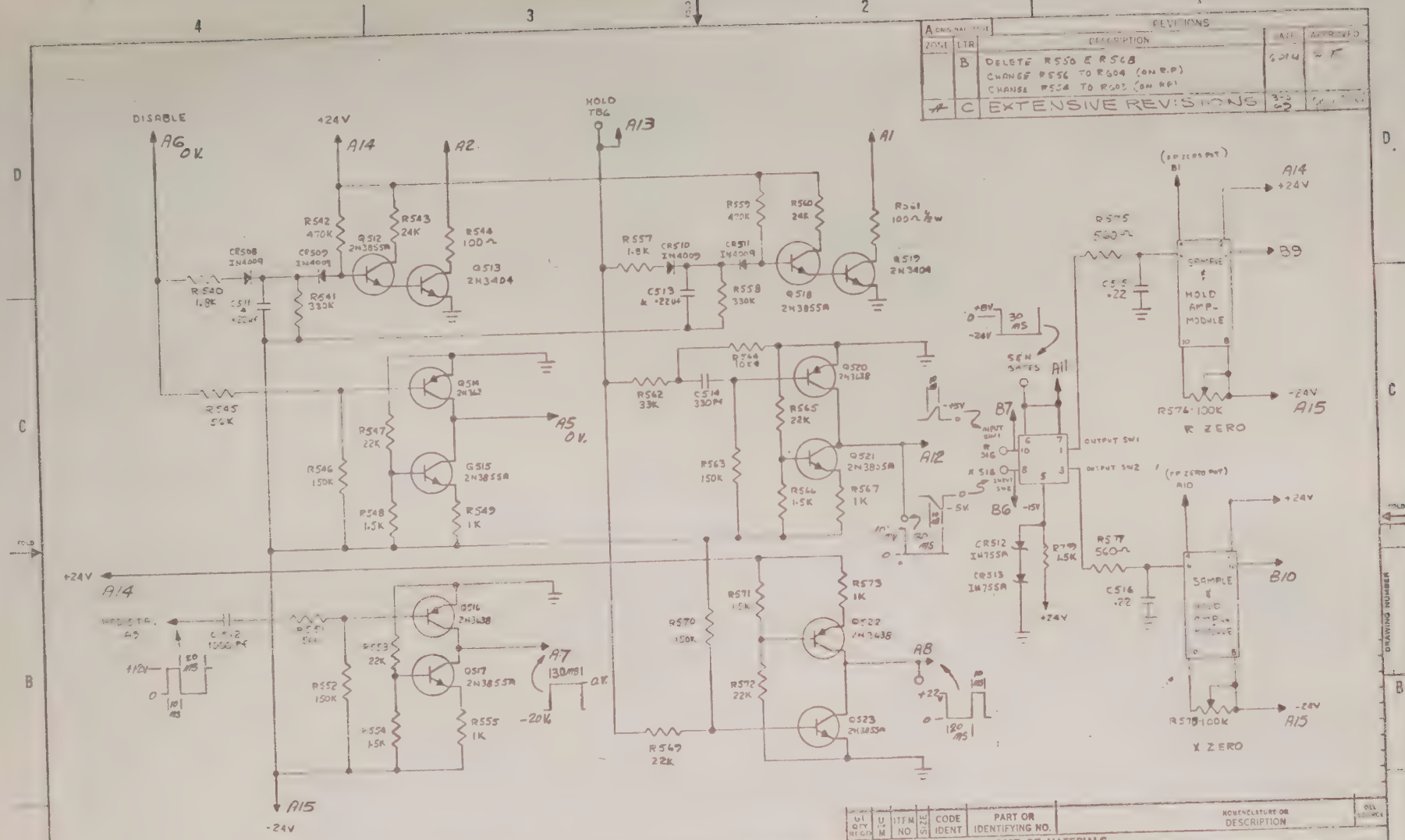
FINISH

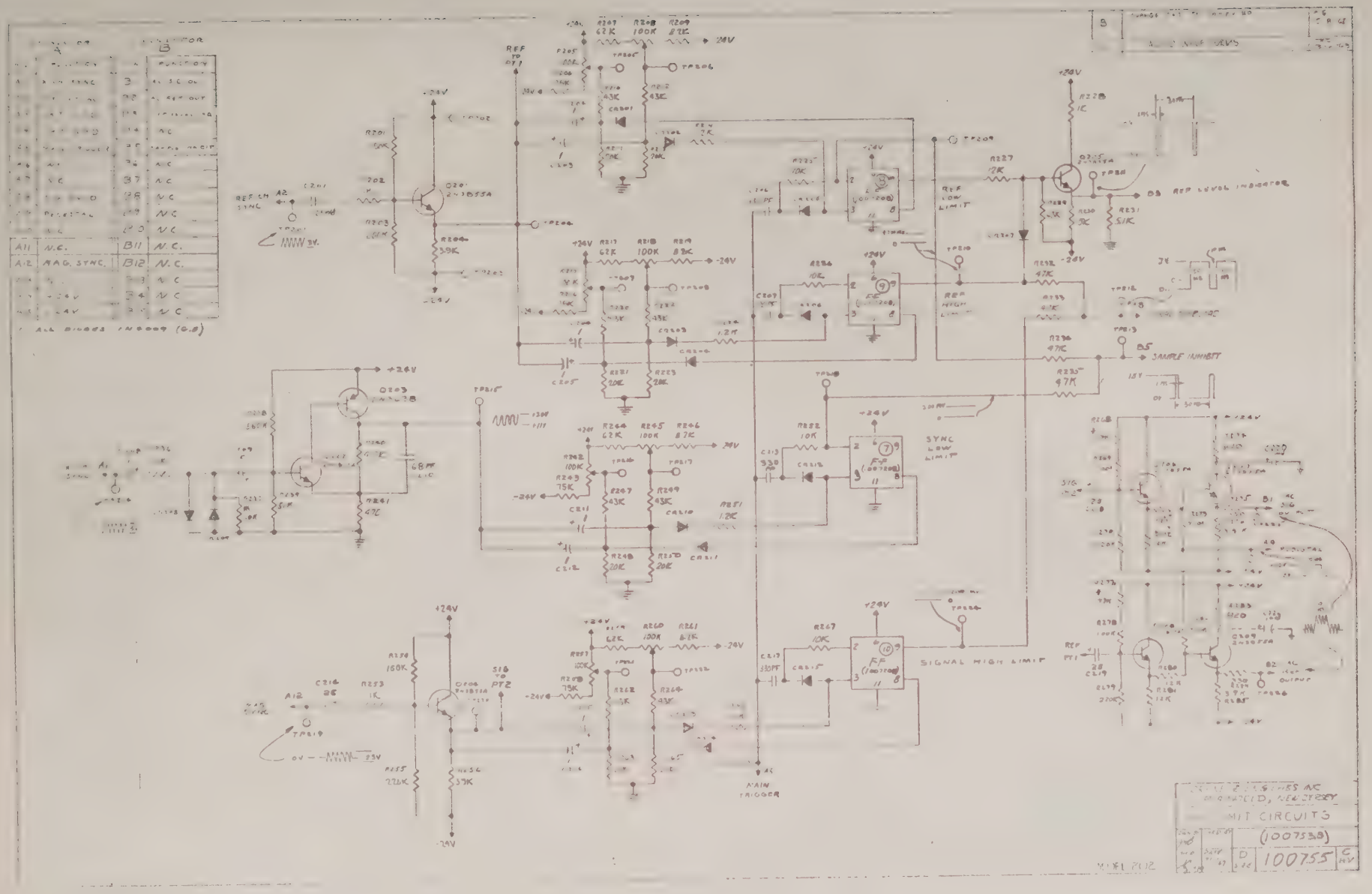
BASIC DIMENSION	DECIMALS 2 PLACE	3 PLACE	FRACTIONS
UNDER 6	± .02	± .005	± 1/64
6 TO 24 INCL	± .03	± .010	± 1/32

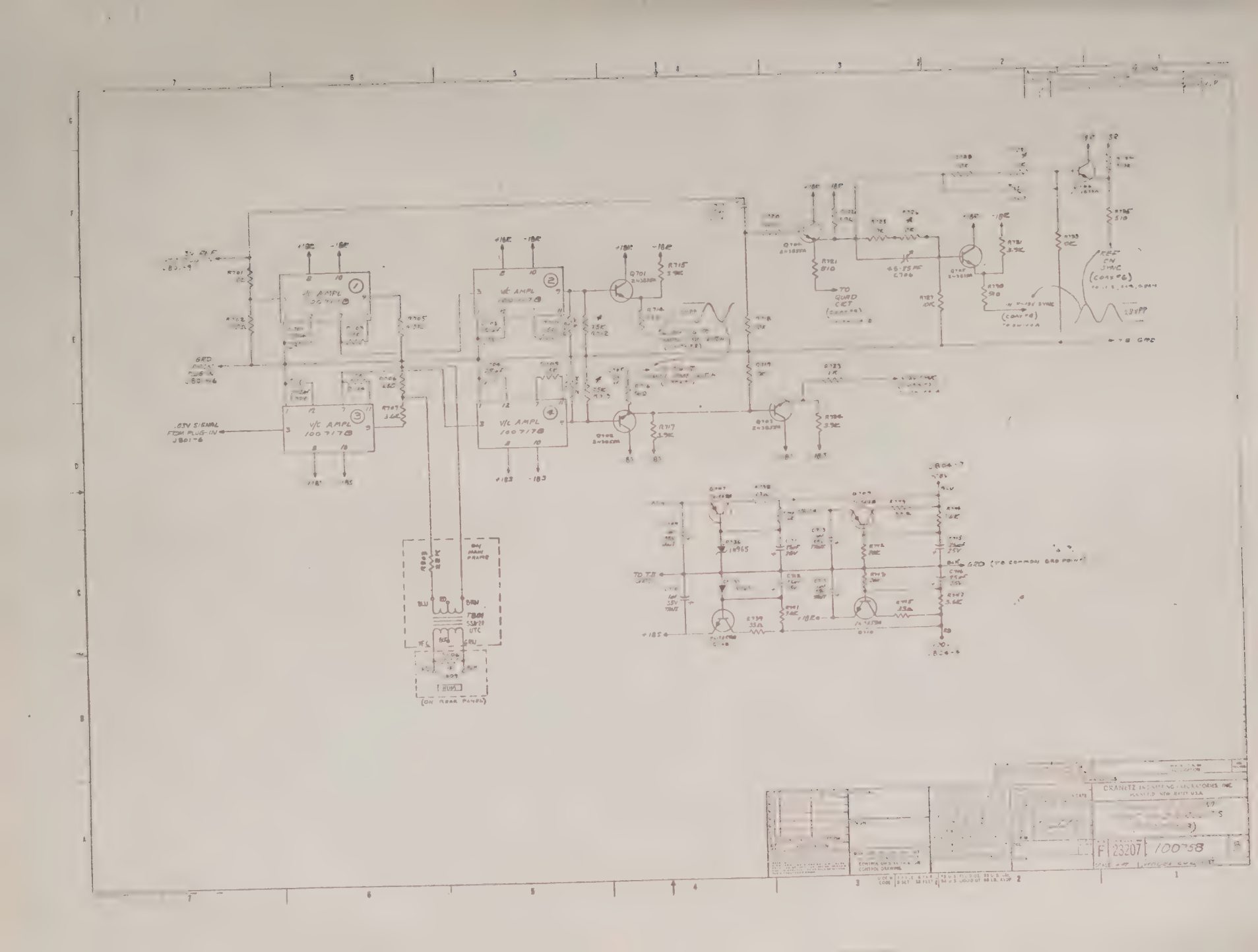
U OF M CODE	1 PIECE	6 PAIR	12 U S FLUID OZ.	53 U S GAL
	5 SET	32 FEET	16 U S LIQUID QT.	68 LB. AVDP

100884 A

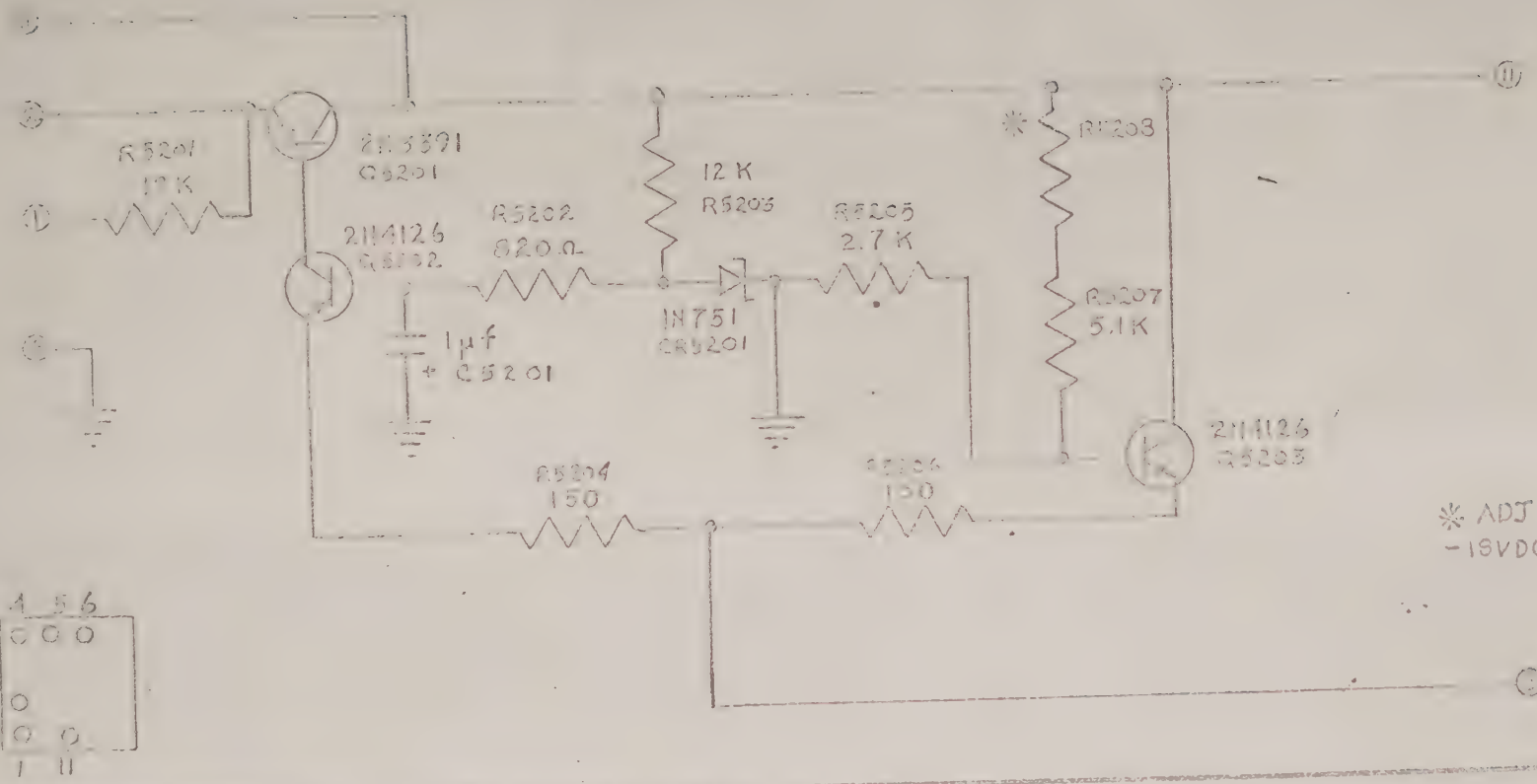
ORIGINAL ISSUE
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED


DISABLE
AG 0V.
+24V
A14
A2
HOLD TB6
A13
A1
R542 470K
R543 24K
R544 100Ω
Q512 2N3855A
Q513 2N3404
CR508 IN4009
CR509 IN4009
R540 1.8K
C511 .22μF
R541 330K
R557 1.8K
CR510 IN4009
CR511 IN4009
C513 .22μF
R559 470K
R560 24K
R558 330K
Q518 2N3855A
R561 100Ω ½W
Q519 2N3404
R545 56K
Q514 2N3638
R546 150K
R547 22K
Q515 2N3855A
R548 1.5K
R549 1K
A5 0V.
R562 33K
C514 330PF
R564 10K
Q520 2N3638
R565 22K
Q521 2N3855A
R563 150K
R566 1.5K
R567 1K
A12
+15V
-15V
B7
B6
INPUT SW1 R SIG
INPUT SW2 R SIG
OUTPUT SW1
OUTPUT SW2
A11
SEQ'N SAMPLES
+8V
-24V
30 MS
5K
10K
20 MS
(2P ZERO PAT)
B1
A14
+24V
R575 560Ω
C515 .22
SAMPLE & HOLD AMP-MODULE
B9
R576 100K
R ZERO
-24V
A15
CR512 IN755A
CR513 IN755A
R569 4.5K
R577 560Ω
C516 .22
(1P ZERO PAT)
A10
B10
R578 100K
X ZERO
+24V
A14
INPUT SIG. A9
C 512 1000 PF
R551 56K
R553 22K
Q516 2N3638
Q517 2N3855A
R552 150K
R554 4.5K
R555 1K
A7
130 MS
0V.
-20K
R570 150K
R571 15K
R573 1K
Q522 2N3638
R572 22K
Q523 2N3855A
A8
+22V
120 MS
R569 22K
-24V
A15
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B | DELETE R550 & R568; CHANGE R556 TO R604 (ON R.P.); CHANGE R554 TO R603 (ON R.P.)
C | EXTENSIVE REVISIONS
LIST OF MATERIALS
QUANTITY NEXT ASSY | U/M | ITEM NO | SIZE | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | SEE SOURCE
DRANETZ ENGINEERING LABORATORIES INC
PLAINFIELD NEW JERSEY USA
TIMING & OUTPUT UNITS
SCHEMATIC DIAGRAM
SIZE C | 23207 | REV C
SCALE none | MODEL 202 | SHEET 2 OF 2
MATERIAL
FINISH
NEXT ASSEMBLY | USED ON
APPLICATION
DIMENSION | 2 PLACE | 3 PLACE | FRACTIONS
6-24 INCL | ± .03 | ± .010 | ± 1/64
OVER 24 | ± .06 | ± .015 | ± 1/16
UNLESS OTHERWISE SPECIFIED
CONTRACT
APPROVALS SIGNATURE & DATE
DRAWN
TRACED
CHECKED
ENGR
PROJ ENGR
MFG
QUALITY
DEL
OTHER
DO NOT SCALE DRAWING
WITHIN .XXX NO CLOSER TOLERANCE
VENDOR ITEM, SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING.
U/M: 1 PIECE 6 PAIR 5 SET 32 FEET
2 U.S. FLUID OZ 55 U.S. GAL 4 U.S. LIQUID QT. 68 LB. AVDP


MAIN TRIGGER
SYNC LOW LIMIT
SIGNAL HIGH LIMIT
REF LOW LIMIT
REF HIGH LIMIT
B5 REF LEVEL INDICATOR
B5 SAMPLE INHIBIT
MIT CIRCUITS
(100738)
100755

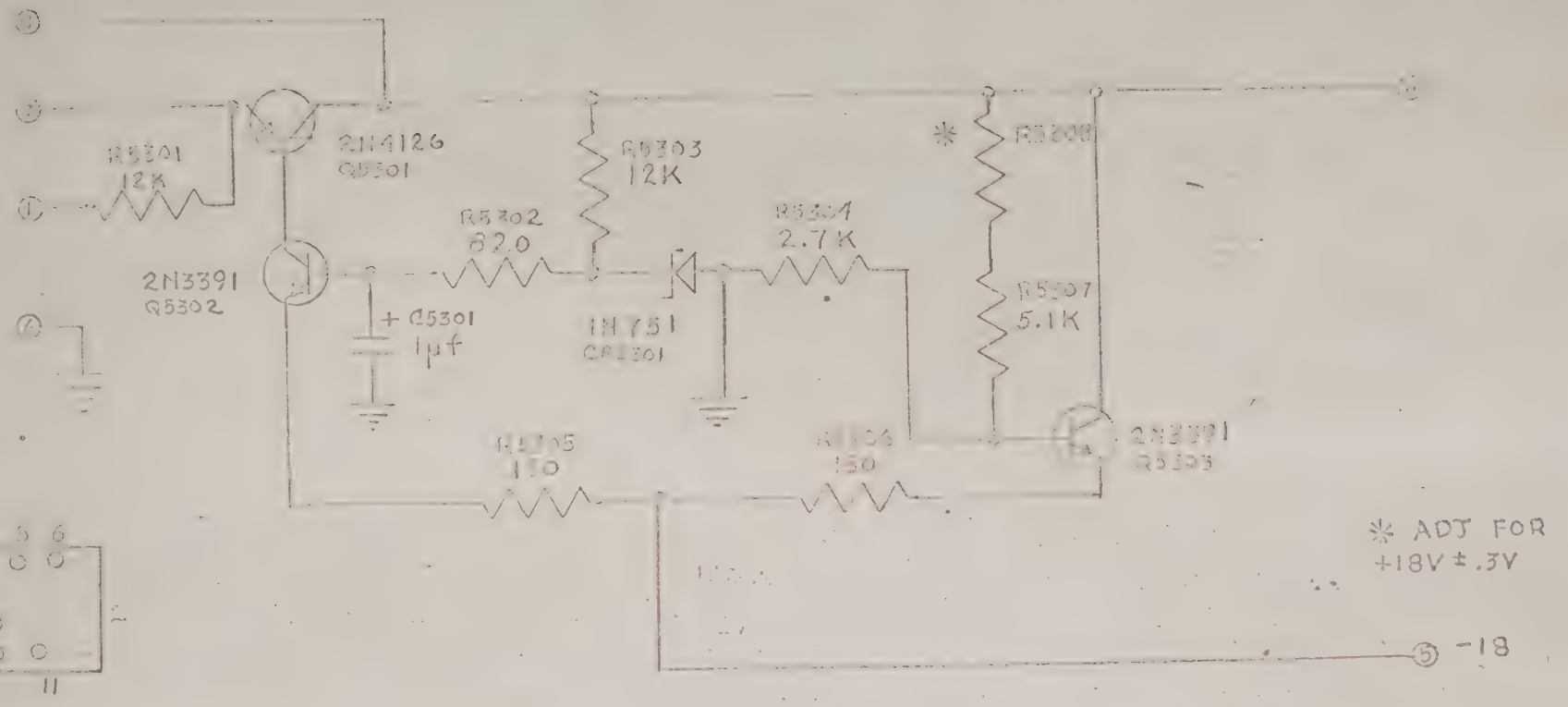

V/C AMPL
100717
(1)
(2)
(3)
(4)
+18V
-18V
+18
-18
GRID
SIGNAL
FROM PLUG-IN
J80116
+18V
-18V
+18
-18
TO QUAD CKT
(CONT'D)
(CONT'D)
(CONT'D)
TO J80116A
TO J80116A
TO J80116A

LTR	DESCRIPTION	DATE	APPROVED



	UNLESS OTHERWISE SPECIFIED	CONTR	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A.
	DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	DWN	REGULATOR -16VDC
		CKD	
		APPD	
	COML. TOL. APPLY TO STOCK SIZES	DFT	SIZE A — CONTRACT NO. 23207 — DRAWING NO. A01152
NEXT ASSY	USED ON	FRACTION ± 1/64 3 PLACE ± .005	SHEET
APPLICATION			

CONTROLS CORP., BROOKLYN, N. Y. 11217 REPROVELL NO. 440M

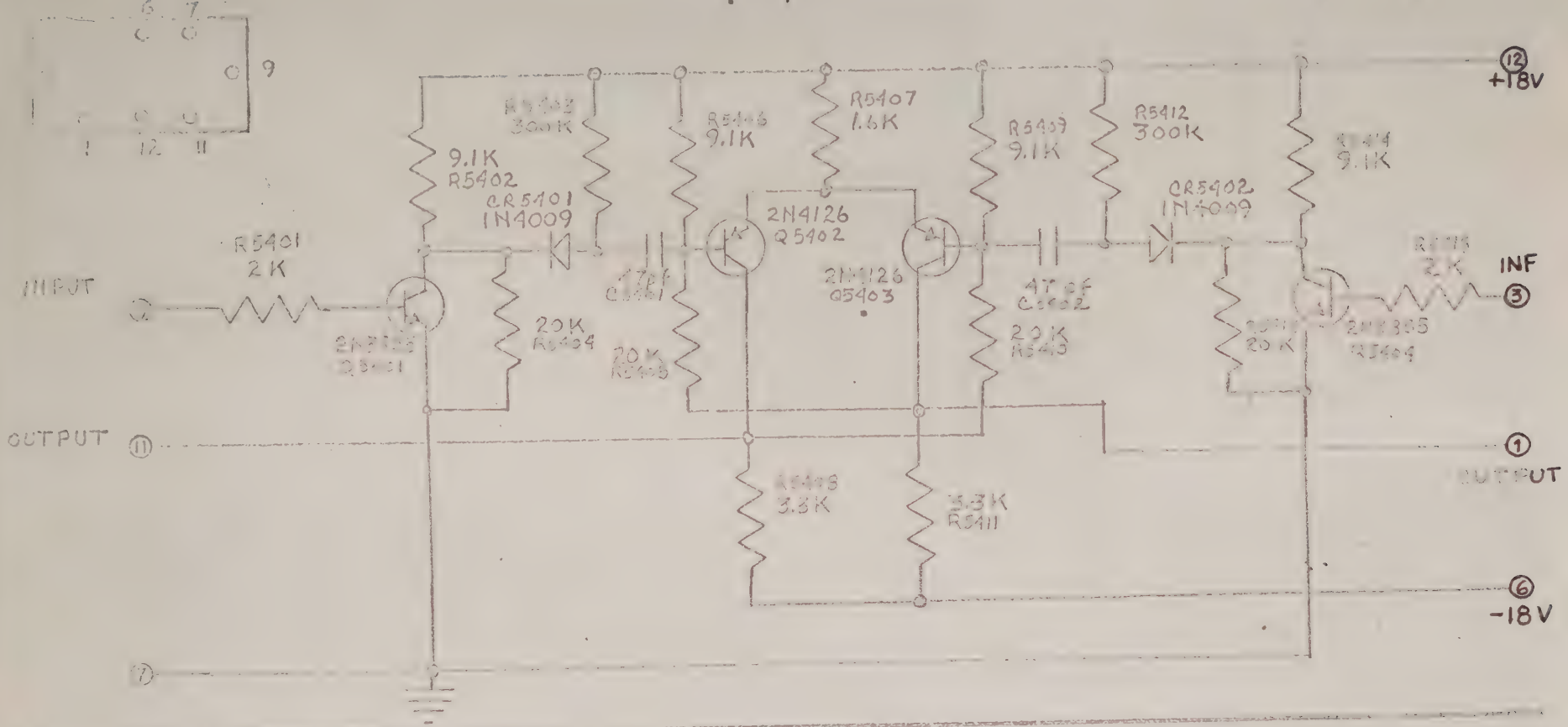


			UNLESS OTHERWISE SPECIFIED	CONTR	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A.
			DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	DWN	
				CKD	
				APPD	REGULATOR +18 VDC
			COML. TOL. APPLY TO STOCK SIZES		
				DFT.	SIZE A / COMPONENT NO. 23207 / 101163
NEXT ASSY	USED ON	DS	FRACTION ± 1/64 3 PLACE ± .005		SHEET
APPLICATION					

GROUP C1 G G

ROBINS GOTTHOLD CORP., BROOKLYN, N.Y. 11217 REMOVAL NO. 440M

LTR	DESCRIPTION	DATE	APPROV



		UNLESS OTHERWISE SPECIFIED	CONTR
		DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	DWN
		COML. TOL. APPLY TO STOCK SIZES	CKD
		FRACTION ± 1/64 3 PLACE ± .005	APPD
			DEL

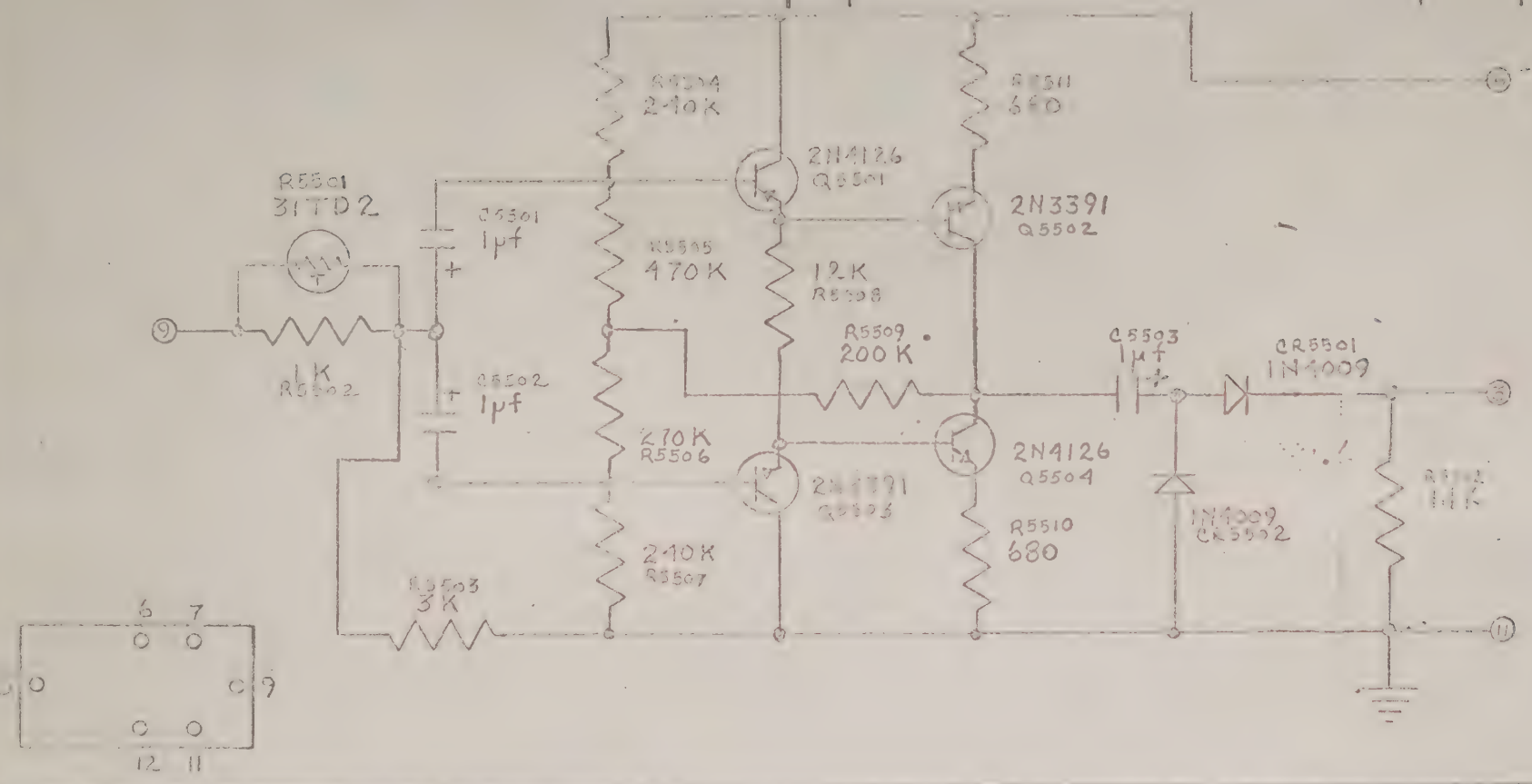
DRANETZ ENGINEERING LABORATORIES, INC.
PLAINFIELD, NEW JERSEY U.S.A.

DIFFERENTIATOR & Ø METER F.F.

SIZE	CUSTOMER DWG. NO.	DRANETZ DWG. NO.
A	23207	101151

SHEET

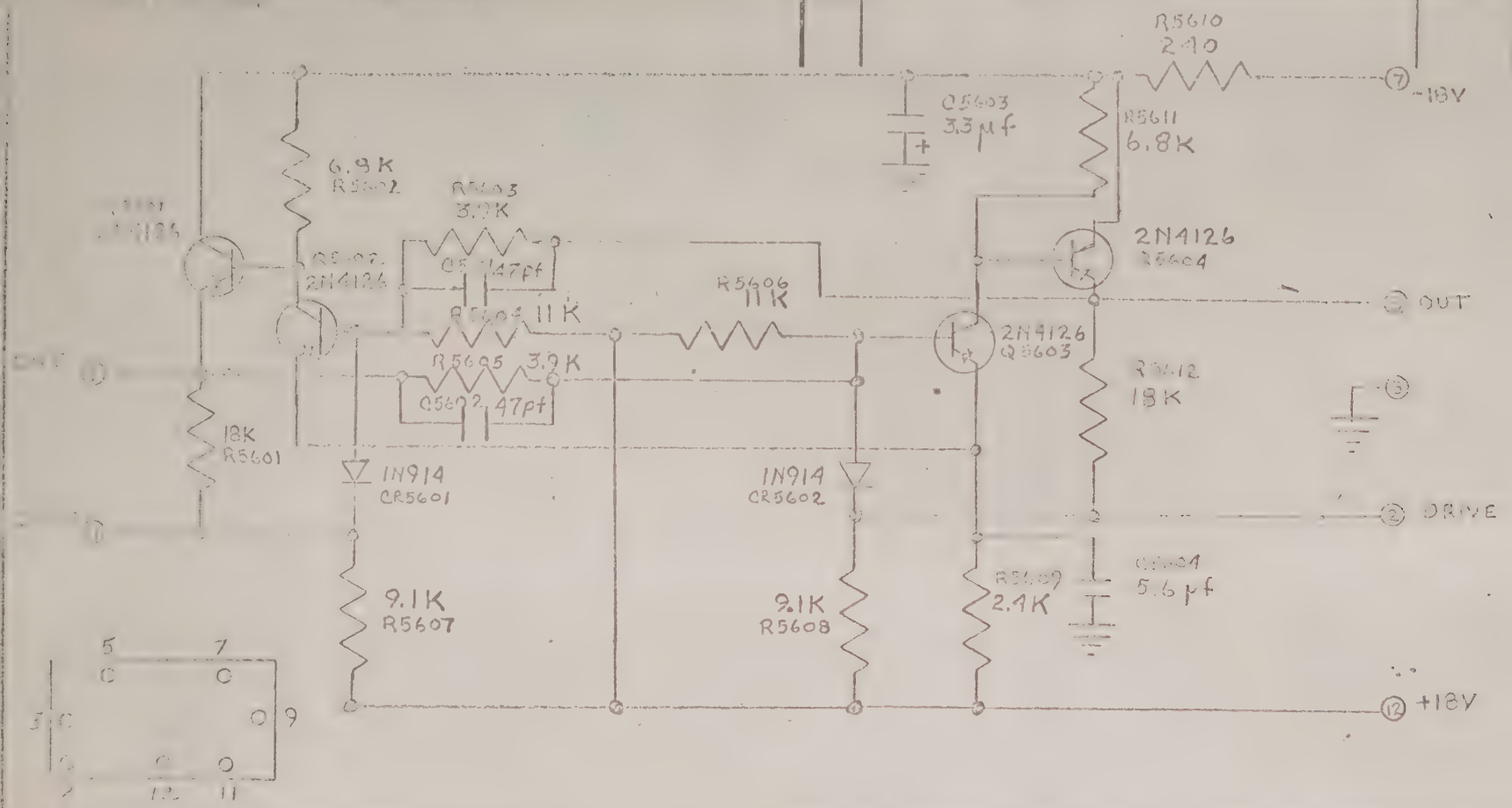
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	CONTR	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD NEW JERSEY U.S.A.	
	DWN		
	CKD		
	APPD	DETECTOR	
COML. TOL. APPLY TO STOCK SIZES			
FRACTION ± 1/64 3 PLACE ± .005	DEL	SIZE A / CODE IDENT. NO. 23207 / 101155	
APPLICATION			SHEET

... CONTROLS CORP., BROOKLYN, N. Y. 11217 REPRODUCE NO. 440M

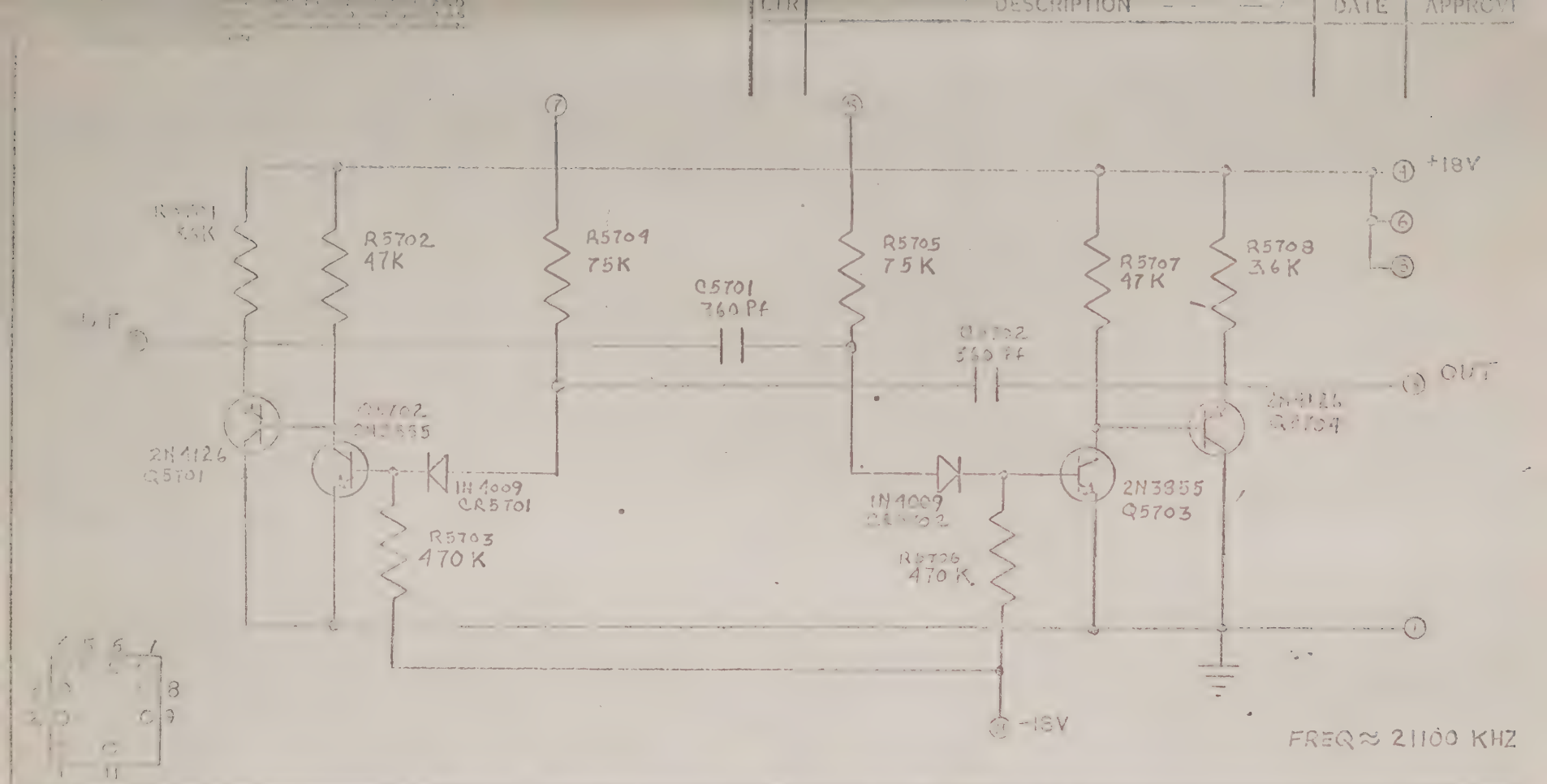
LTR	DESCRIPTION	DATE	APPROVE



	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	CONTR	DRANETZ ENGINEERING LABORATORIES INC. PLAINFIELD, NEW JERSEY U.S.A.
		DWN	
		CKD	CHOPPER DRIVER & ÷BY2
		APPD	
	COML. TOL. APPLY TO STOCK SIZES	DEL	
	FRACTION ± 1/64 3 PLACE ± .005		SIZE A | CODE IDENT. NO. 23207 | 101156
			SHEET

APPLICATION

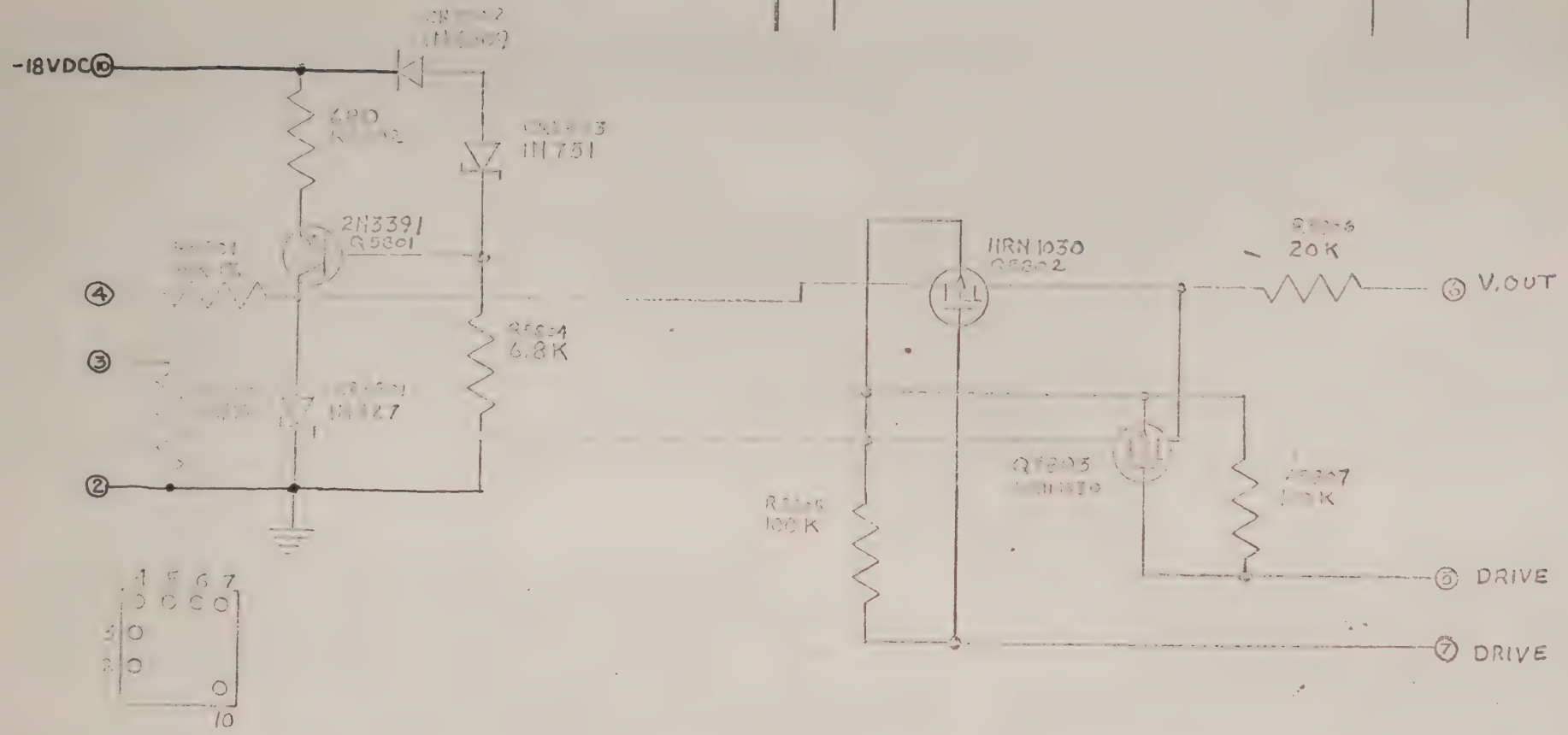
APPROVED NO. 440M



		UNLESS OTHERWISE SPECIFIED	CONTR	DRANETZ [illegible] LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A.	
		DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	DWN		
			CKD		
			APPD	OSCILLATOR	
		COML. TOL. APPLY TO STOCK SIZES			
NEXT ASSY	USED ON DS	FRACTION ± 1/64 3 PLACE ± .005	DEL	SIZE A	CODE IDENT. NO. 23207
APPLICATION					SHEET

[illegible] CONTROLS CORP., BROOKLYN, N. Y. 11217 REPROVEL NO. 440M

LTR	DESCRIPTION	DATE	APPROVED

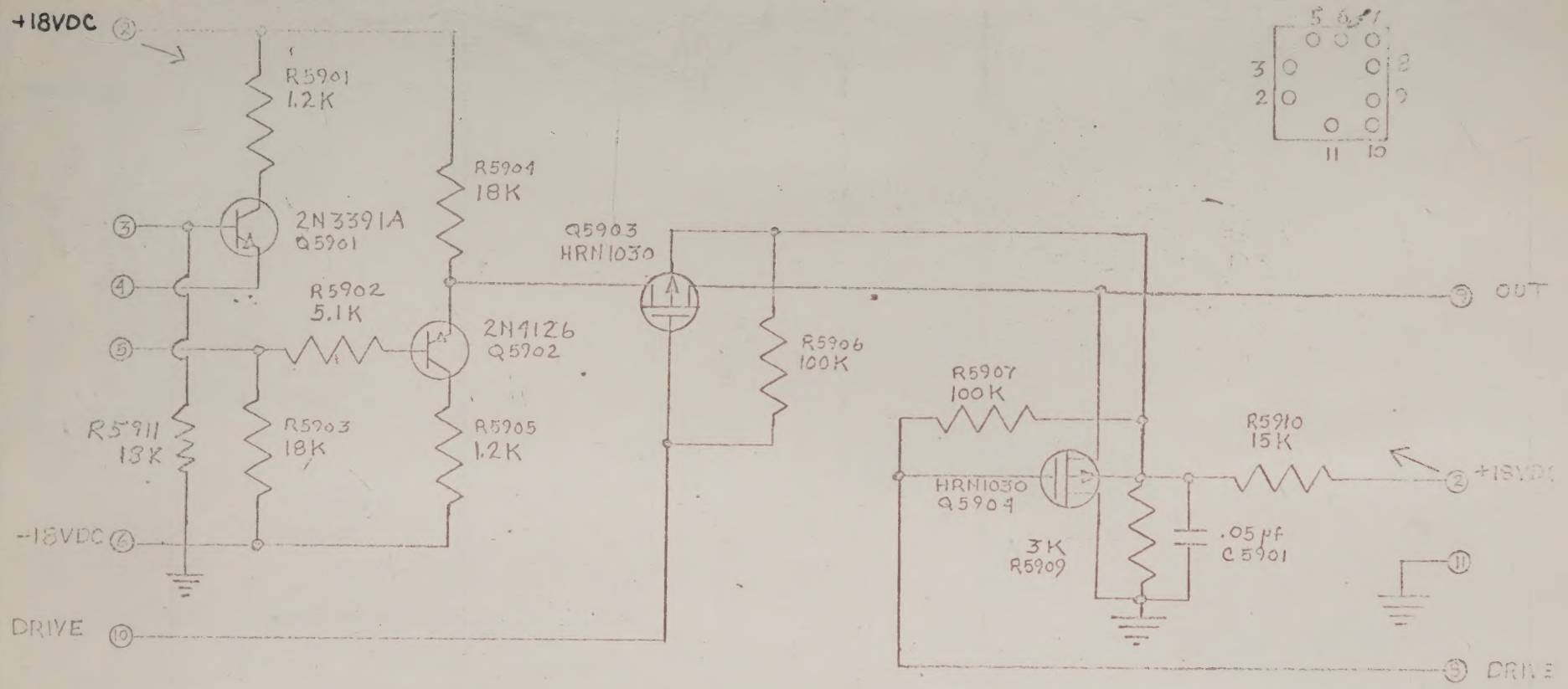


	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES COML. TOL. APPLY TO STOCK SIZES FRACTION ± 1/64 3 PLACE ± .005	CONTR DWN CKD APPD DEL	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A. Ø METER SWITCH & REFERENCE SOURCE SIZE A | CODE IDENT. NO. 23207 | 101153 SHEET

APPLICATION

BROOKLYN, N. Y. 11217 REPROVELL NO. 440M

SHALL NOT BE REPRODUCED, OR COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT PERMISSION.



G			UNLESS OTHERWISE SPECIFIED	CONTR	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A.
G				DWN	
G			DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	CKD	INPUT STAGE & CHOPPER (2 REQ)
G				APPD	
G			COML. TOL. APPLY TO STOCK SIZES		
G1				DEL	SIZE A | CODE IDENT. NO. 23207 | 101159
GROUP	NEXT ASSY	USED ON DS	FRACTION ± 1/64 3 PLACE ± .005		SHEET
	APPLICATION				

GRAPHIC CONTROLS CORP., BROOKLYN, N. Y. 11217 REPROVEL NO. 440M

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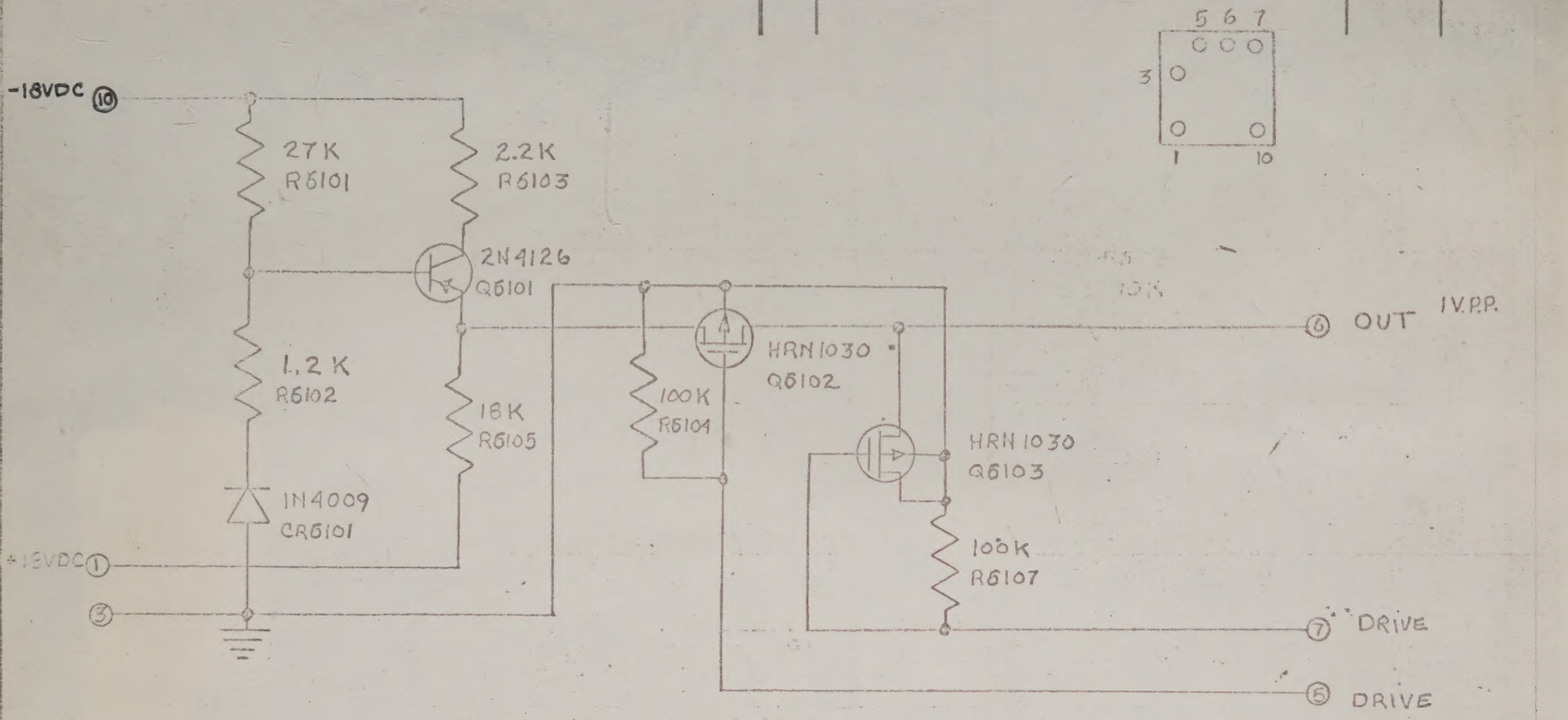
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVE
	ORIGINAL ISSUE		



G			UNLESS OTHERWISE SPECIFIED	CONTR	DRANETZ ENGINEERING LABORATORIES, INC. PLAINFIELD, NEW JERSEY U.S.A.
G				DWN	
G			DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	CKD	VOLTAGE SOURCE & CHOPPER (REF.)
G				APPD	
G					
G1			COML. TOL. APPLY TO STOCK SIZES	DEL	SIZE A | CODE IDENT. NO. 23207 | 101 161
GROUP	NEXT ASSY	USED ON DS	FRACTION ± 1/64 3 PLACE ± .005		SHEET
	APPLICATION				

MP MASTER
MA22485